```
     FILE 'REGISTRY' ENTERED AT 16:50:27 ON 23 MAY 2002
L1           18 S C4F8/MF
L2           15 S C4F6/MF
L3           18 S C5F8/MF
L4            9 S CF4/MF
L5            6 S C2F6/MF
L6            3 S C3F8/MF
L7           35 S H3N/MF

     FILE 'HCAPLUS' ENTERED AT 16:51:39 ON 23 MAY 2002
                E FLUOROCARBON/CT
                E FLUOROCARBONS/CT
                E E3+ALL/CT
L8         5692 S E1-2
L9         7666 S L8 OR (FLUORCARBON OR (CARBON FLUORIDE))
                E AMMONIA/CT
                E E3+ALL/CT
L10      147235 S AMMONIA
L11          67 S L7 AND L1
L12      260577 S (DIELECTRIC OR INSULAT? OR OXIDE)(3N)(LAYER OR FILM OR COAT##
L13          16 S L11 AND L12
L14          11 S L7 AND L2
L15           3 S L7 AND L3
L16         436 S L7 AND L4
L17          66 S L16 AND L12
L18          52 S L17 AND ETCH?
L19          76 S L16 AND L5
L20          17 S L19 AND L12
L21           1 S L20 NOT (L13-15 OR L18)
L22          10 S L14 NOT L13
L23           2 S L15 NOT (L13 OR L14)
L24          40 S L18 NOT (L13 OR L14 OR L15)
L25           1 S L20 NOT (L13 OR L14 OR L15 OR L18)
L26          61 S L7 AND L6
L27          10 S L26 AND L12
L28           0 S L27 NOT (L13 OR L14 OR L15 OR L18 OR L25)
L29          69 S L13 OR L14 OR L15 OR L18 OR L25 OR L20
L30         195 S (L7 OR NH3 OR L10) AND (L8 OR L9)
L31          30 S L30 AND L12
L32          11 S L31 NOT L29
L33         186 S (NH3 OR L10) AND (L8 OR L9)
L34          49 S L33 AND ETCH?
L35          50 S L30 AND ETCH?
L36         231 S NH3 AND (C4F6 OR C4F8 OR C5F8 OR CF4 OR C2F6 OR C3F8)
L37          22 S L36 AND L12
L38          11 S L37 NOT (L29 OR L32)
```

L13 ANSWER 1 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:241319 HCAPLUS
DN 136:271749
TI Etching method for a silicon carbide film
IN Nishizawa, Atsushi
PA NEC Corporation, Japan
SO U.S. Pat. Appl. Publ., 13 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 2002037648 | A1 | 20020328 | US 2001-950769 | 20010913 |
| JP 2002110644 | A2 | 20020412 | JP 2000-295905 | 20000928 |
| PRAI JP 2000-295905 | A | 20000928 | | |

AB A dry etching method, with a gas contg. N added to an etching gas contg. a halogen compd. for an SiC **film**, applies a low **dielec.** const. **film** to an interlayer **insulating film** and reduces parasitic capacitance between groove wirings. In manufg. of a multilayer wiring structure, an SiC **layer** and an interlayer **insulating film** are laminated on a lower layer wiring, and a via hole that reaches the surface of the SiC layer and a wiring groove is formed by dry-etching a region of the interlayer **insulating film**. The exposed SiC layer is then removed by dry etching, using the interlayer **insulating film** as an etching mask, and the via hole penetrates the SiC layer to the surface of the lower layer wiring. The penetrating via hole and the wiring groove are filled with a conductive material to form a groove wiring connecting with the lower layer wiring.

L13 ANSWER 2 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:11081 HCAPLUS
DN 136:78346
TI Fabrication method of semiconductor integrated circuit device
IN Tadokoro, Masahiro; Shioya, Masahiro; Kojima, Masayuki; Ikeda, Takenobu
PA Japan
SO U.S. Pat. Appl. Publ., 67 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 2002001963 | A1 | 20020103 | US 2001-893577 | 20010629 |
| JP 2002025979 | A2 | 20020125 | JP 2000-200986 | 20000703 |
| PRAI JP 2000-200986 | A | 20000703 | | |

AB A fabrication method of a semiconductor integrated circuit device comprises, in an SAC process or HARC process, subjecting a semiconductor substrate to plasma etching to make contact holes in an **oxide film** made of a Si **oxide film** formed on the semiconductor substrate. For improving the ease-in-etching property of the Si **oxide film** and selectivity to a nitride film, a residence time of an etching gas within a chamber is so set as to be in a range where selectivity to an **insulating film** made of Si nitride is improved by using etching conditions of a low pressure and a large flow rate of the etching gas of C5H8/O2/Ar.

L13 ANSWER 3 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:828984 HCAPLUS
DN 135:351560
TI Inter-metal **dielectric film** composition for dual damascene process for fabrication of integrated circuits with reduced resistance and capacitance of the interconnect
IN Chen, Dian-hau; Ma, Ching-tien; Lee, Hsiang-tan
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 6316351 | B1 | 20011113 | US 2000-583399 | 20000531 |
| | US 2002013024 | A1 | 20020131 | US 2001-972646 | 20011009 |
| PRAI | US 2000-583399 | A3 | 20000531 | | |

AB The use of an intermetal **dielec**. (IMD) **layer** and an org. etch-stop layer are disclosed in forming a dual damascene to reduce the RC delay and the overall dielec. const. of the damascene interconnect. The disclosed IMD layer is an FSG and the etch-stop layer is an org. spin-on-glass (SOG). A dual damascene structure using the IMD layer and the org. etch-stop layer is also disclosed.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 4 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:336818 HCAPLUS
DN 134:335280
TI Fabrication of semiconductor device
IN Sato, Kiyoyuki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 2001127039 | A2 | 20010511 | JP 1999-302329 | 19991025 |

AB The title method involves forming a multilayer film of a nitride bottom **layer** and **oxide** top **layer** on a substrate, selectively etching the **oxide** top **layer** using a first etching gas to from an opening, and etching the nitride bottom layer via the opening using a second etching gas based on CxFy such as C3F6, C4F6, C4F8, or C5F8. Addnl., the second etching gas may contain CH2F2, CH3F, CH3Br, NH3, EtOH, MeOH, CO, or CO2. The etching selectivity is improved. The method is useful for forming contact holes.

L13 ANSWER 5 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:210341 HCAPLUS
DN 134:230802
TI Apparatus and method for plasma processing
IN Yokokawa, Katanobu; Izawa, Masaru; Itabashi, Naoshi; Yamamoto, Seiji; Taji, Shinichi; Negishi, Nobuyuki; Takahashi, Nushito
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF

DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 2001077090 | A2 | 20010323 | JP 1999-249639 | 19990903 |

AB The title method involves forming a plasma by the interaction between an electromagnetic wave of 300-500 MHz and a magnetic field, applying an electromagnetic wave of 50-30 MHz on an electromagnetic-wave-introduction plate while superimposing on the electromagnetic wave of 300-500 MHz, and maintaining a certain spacing between the plate and substrate to be processed. The active species in the plasma are effectively controlled independent from the plasma-generation conditions for stable processing for a long period of time. An app. for carrying out the above method is also described. The method and app. are useful for plasma etching of an **insulator film** in semiconductor device fabrication.

L13 ANSWER 6 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:62455 HCAPLUS
DN 134:124647
TI Dry etching method for forming tungsten and tungsten compound wiring of arbitrary taper angle in a semiconductor device
IN Suzawa, Hideomi; Ono, Koji
PA SEL Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 32 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| EP 1071124 | A2 | 20010124 | EP 2000-115333 | 20000714 |
| EP 1071124 | A3 | 20011024 | | |
| R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO | | | | |
| JP 2001035808 | A2 | 20010209 | JP 1999-206954 | 19990722 |
| CN 1282107 | A | 20010131 | CN 2000-121738 | 20000724 |
| PRAI JP 1999-206954 | A | 19990722 | | |

AB A dry etching method for forming W wiring having a tapered shape and having a large specific selectivity with respect to a base film is provided. If the bias power d. is suitably regulated, and if desired portions of a W thin film are removed using an etching gas having F as its main constituent, then the W wiring having a desired taper angle can be formed. The W and tungsten compd. wirings are gate wirings of thin film transistor. The semiconductor devices are active matrix liq. crystal display devices, EL display devices, and electronic appliances.

L13 ANSWER 7 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:830370 HCAPLUS
DN 133:368487
TI Method to increase the coupling ratio of word line to floating gate by lateral coupling in stacked-gate flash memory
IN Hsieh, Chia-Ta; Kuo, Di-Son; Lin, Yai-Fen; Lin, Chrong Jung; Chen, Jong; Su, Hung-Der
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English

FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6153494 | A | 20001128 | US 1999-310257 | 19990512 |

AB A method is provided for forming a stacked-gate flash memory cell having a shallow trench isolation with a high-step of oxide and high lateral coupling. This is accomplished by 1st depositing an unconventionally high or thick layer of nitride and then forming a shallow trench isolation (STI) through the nitride layer into the substrate, filling the STI with isolation oxide, removing the nitride thus leaving behind a deep opening about the filled STI, filling conformally the opening with a 1st polysilicon layer to form a floating gate, forming interpoly **oxide layer** over the floating gate, and then forming a 2nd polysilicon layer to form the control gate and finally forming the self-aligned source of the stacked-gate flash memory cell of the invention. A stacked-gate flash memory cell is also provided having a shallow trench isolation with a high-step of oxide and high lateral coupling.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 8 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:490797 HCAPLUS
DN 133:82921
TI Method to fabricate sharp tip of polysilicon in split gate flash memory
IN Lin, Yai-Fen; Hsieh, Chia-Ta; Sung, Hung-Cheng; Yeh, Jung-Ke; Lin, Chang-Song; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English

FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6090668 | A | 20000718 | US 1999-248725 | 19990211 |

AB A method is provided for forming a split-gate flash memory cell having a sharp poly tip which substantially improves the erase speed of the cell. The poly tip is formed without the need for conventional oxidn. of the polysilicon floating gate. Instead, the polysilicon layer is etched using a high pressure recipe thereby forming a recess with a sloped profile into the polysilicon layer. The recess is filled with a top-oxide, which in turn serves as a hard mask in etching those portions of the polysilicon year not protected by the top-**oxide layer**. The edge of the polysilicon layer formed by the sloping walls of the recess forms the sharp poly tip of this invention. The sharp tip does not experience the damage caused by conventional poly oxidn. processes and, therefore, provides enhanced erase speed for the split-gate flash memory cell. The invention is also directed to a semiconductor device fabricated by the disclosed method.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 9 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:457321 HCAPLUS
DN 133:67307
TI Method of plasma etching silica using hydrogen-containing additive gases in fluorocarbon gas chemistry
IN Hills, Graham; Nguyen, Thomas; Keil, Douglas; Khajehnouri, Keyvan
PA Lam Research Corp., USA

SO PCT Int. Appl., 26 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI WO 2000039846 | A1 | 20000706 | WO 1999-US31077 | 19991228 |
| W: IL, JP, KR, SG | | | | |
| RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE | | | | |
| US 6217786 | B1 | 20010417 | US 1998-223963 | 19981231 |
| EP 1147549 | A1 | 20011024 | EP 1999-968192 | 19991228 |
| R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI | | | | |

PRAI US 1998-223963 A 19981231
WO 1999-US31077 W 19991228
AB A method of etching an **oxide layer** in a plasma etching reactor is disclosed. The method includes the steps of providing a semiconductor substrate including the **oxide layer** into the plasma etching reactor and flowing an etching gas that includes a fluorocarbon gas, a N reactant gas, an O reactant gas, an inert carrier gas, and a H-contg. additive gas into the plasma etching reactor. The method further includes etching an opening at least partially through the **oxide layer** using a plasma that is formed from the etching gas.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 10 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:454271 HCAPLUS
DN 133:52302
TI Borderless contact and via fabrication for semiconductor devices
IN Tsai, Chao-Chieh; Ho, Chin-Hsiung; Sun, Yuan-Chen
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6083824 | A | 20000704 | US 1998-114132 | 19980713 |

AB A method of forming borderless contacts and vias is disclosed. Borders which are conventionally provided in aligning contacts and vias to device and/or metal regions in a semiconductor device take up too much valuable real estate on semiconductor substrates, and hence reduce productivity of the products. By employing a hard-mask of this invention, and a specific sequence of process steps, alignment can be achieved without the need for borders. First, a thin nitride layer is deposited on an **insulating layer** formed over a substructure of a substrate having device and/or metal regions. The hard-mask is patterned with metal line openings, and a photoresist layer is formed with contact or via pattern over the already patterned hard-mask. The contact/via openings are etched into the **dielec. layer** until the substructure is reached. The hole openings are filled plug metal and then partially etched back, leaving a plug in the hole opening. The line trench is etched further into the **dielec. layer** until metal plug is reached. The trench is then filled with metal, such as

Al-Cu or Cu and the excess is removed by chem.-mech. polishing. Thus, a borderless and self-aligned interconnect comprising plug and metal line is formed.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 11 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:321510 HCAPLUS
DN 132:316774
TI High selectivity etching stop layer for damascene process in semiconductor device fabrication
IN Chao, Li-chih; Tsai, Chia-shiung; Fu, Chu-yun; Liaw, Jhon-jhy
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6063711 | A | 20000516 | US 1998-69456 | 19980428 |

AB A high selectivity etch-stop layer comprising oxynitride is disclosed for forming damascene structures in the manufg. of semiconductor substrates. Because of its relatively high selectivity to oxides, the oxynitride etch-stop can be made thinner than the conventionally used nitride layer. Therefore, the disclosed oxynitride etch-stop layer makes it possible to avoid the cracking problems of thicker etch-stop layers as well as the assocd. problems of poor definition of contact or via holes in the damascene structure.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 12 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:631313 HCAPLUS
DN 129:269049
TI Selective etching of dielectrics using fluorohydrocarbon gas, NH3-generating gas, and carbon-oxygen gas
IN Ding, Ji; Shan, Hongching; Welch, Michael
PA Applied Materials, Inc., USA
SO U.S., 13 pp., Cont.-in-part of U. S. Ser. No. 639,388.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 5814563 | A | 19980929 | US 1996-660966 | 19960612 |
| US 5843847 | A | 19981201 | US 1996-639388 | 19960429 |
| JP 10041274 | A2 | 19980213 | JP 1997-112887 | 19970430 |
| JP 10056001 | A2 | 19980224 | JP 1997-147995 | 19970605 |
| EP 813233 | A2 | 19971217 | EP 1997-304035 | 19970610 |
| EP 813233 | A3 | 19990825 | | |

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI

| | | |
|---|---|---|
| PRAI US 1996-639388 | 19960429 | |
| US 1996-660966 | 19960612 | |

AB A method of etching a **dielec. layer** on a substrate with high etching selectivity, low etch rate microloading, and high etch rates is described. A substrate having a **dielec. layer**

with resist material on it is placed in a process zone, and a process gas is introduced into the process zone. The process gas comprises (i) fluorohydrocarbon gas for forming F-contg. etchant species capable of etching the **dielec. layer**; (ii) NH3-generating gas having a liquefaction temp. LT of .apprx.-60 to +20.degree.; and (iii) C-O gas. The temp. of the substrate is maintained within about .+-.50.degree. of the LT of the NH3-generating gas. A plasma is formed from the process gas to etch the **dielec. layer** on the substrate. Preferably, the volumetric flow ratio of fluorohydrocarbon:NH3-generating gas is .apprx.2.5:1 to .apprx.7:1.

L13 ANSWER 13 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:298342 HCAPLUS
DN 128:329922
TI Manufacture of semiconductor device involving plasma dry etching of silica film
IN Hata, Kazuhiro; Hirohama, Kazuhiro
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 10125654 | A2 | 19980515 | JP 1996-278232 | 19961021 |

AB The method involves patterning of a SiO2 elec. **insulating film** by dry etching with exited plasma from a F-contg. gas, a N-contg. gas, and an optional Penning effect-inducing inert gas while removing carbon-based deposits formed in the process. Carbon deposits are effectively removed during the etching process.

L13 ANSWER 14 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:13776 HCAPLUS
DN 128:69683
TI Etching a **dielectric layer** using a plasma generated from a mixture of fluorocarbon gas, NH3-generating gas, and a carbon-oxygen-containing gas
IN Ding, Ji; Shan, Hongching; Welch, Michael
PA Applied Materials, Inc., USA
SO Eur. Pat. Appl., 16 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 3

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| EP 813233 | A2 | 19971217 | EP 1997-304035 | 19970610 |
| EP 813233 | A3 | 19990825 | | |
| R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI | | | | |
| US 5814563 | A | 19980929 | US 1996-660966 | 19960612 |
| PRAI US 1996-660966 | | 19960612 | | |
| US 1996-639388 | | 19960429 | | |

AB A method of etching a **dielec. layer** on a substrate with high selectivity, low etch rate microloading, and high etch rates is described. A substrate having a **dielec. layer** with resist material on it is placed in a process zone, a process gas is introduced into the process zone, and a plasma is formed from the process

gas to etch the **dielec. layer** on the substrate. The process gas comprises (i) fluorocarbon gas for forming F-contg. etchant species capable of etching the **dielec. layer**; (ii) NH3-generating gas having a liquefaction temp. of .apprx.-60.degree. to .apprx.20.degree., and (iii) oxycarbon gas contg. C and O bonded to each other. The temp. of the substrate is maintained within about .+-.50.degree. of the liquefaction temp. of the NH3-generating gas.

L13 ANSWER 15 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:651035 HCAPLUS
DN 127:340514
TI Plasma etching of silicon **oxide insulating layer** in semiconductor device manufacture
IN Yanagida, Toshiharu
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 09260350 | A2 | 19971003 | JP 1996-62417 | 19960319 |

AB The **insulating layer** (e.g., made of SiO2, SiOxFz, SiOxNyFz), which is formed on an undercoating layer, is patterned by plasma etching using a mixt. of a N-H gas (e.g., NH3, N2H4, NH4HS) and a C-F gas. Alternatively the etching gas consists of a N-H gas and a S compd. gas to give S radicals to plasma under a discharge condition. The selectivity to the undercoating layer and the resist mask is improved, the microloading effect is small, and the particle level is reduced. The process is esp. useful for contact hole formation.

L13 ANSWER 16 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:290052 HCAPLUS
DN 126:271051
TI Plasma etching in formation of contacts over a silicide layer
IN Van Autryve, Luc
PA Applied Materials, Inc., USA
SO Eur. Pat. Appl., 15 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI EP 763850 | A1 | 19970319 | EP 1996-113955 | 19960830 |
| R: AT, BE, CH, DE, ES, FR, GB, GR, IE, IT, LI, NL, SE | | | | |
| US 5935877 | A | 19990810 | US 1995-522791 | 19950901 |
| JP 09148314 | A2 | 19970606 | JP 1996-251028 | 19960902 |
| PRAI US 1995-522791 | | 19950901 | | |

AB A plasma etch process for an **insulating layer**, such as SiO2, overlying a silicide layer having a high selectivity with respect to the silicide layer is disclosed, comprising the use of a mixt. of a N-contg. gas and .gtoreq.1 other F-contg. etch gases in an etch chamber maintained at .apprx.5-400 millitorr. The high selectivity exhibited by the etch process of the invention permits operation of the etch process at reduced pressures of as low as 5-30 millitorr to achieve complete etching of vertical sidewall openings in the **oxide layer** with significant overetch capability.

L14 ANSWER 1 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:107719 HCAPLUS
DN 136:160067
TI NH3 plasma descumming and resist stripping in semiconductor applications
IN Hsieh, Chang Lin; Chen, Hui; Yuan, Jie; Ye, Yan
PA Applied Materials, Inc., USA
SO PCT Int. Appl., 27 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI WO 2002011193 | A2 | 20020207 | WO 2001-US23992 | 20010731 |
| W: JP, KR, SG | | | | |
| RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR | | | | |
| PRAI US 2000-629329 | A | 20000801 | | |

AB In general, the present disclosure pertains to a method for removing photoresist from locations on a semiconductor structure where its presence is undesired. In one embodiment, a method is disclosed for descumming residual photoresist material from areas where it is not desired after patterning of the photoresist. In another embodiment, a misaligned patterned photoresist is stripped from a semiconductor substrate surface. In particular, the method comprises exposing the semiconductor structure to a plasma generated from a source gas comprising NH3. A substrate voltage was used in both methods to produce anisotropic etching. In the descumming embodiment, the crit. dimensions of the patterned photoresist are maintained. In the photoresist stripping embodiment, a patterned photoresist is removed without adversely affecting a partially exposed underlying layer of an org. dielec.

L14 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:99691 HCAPLUS
DN 136:249349
TI Substitutes for chlorofluorocarbons (CFC) and hydrochlorofluorocarbons (HCFC). Part 2
AU Novari, Giulio
CS Facolta di Economia, Sezione merceologia del Dipartimento di Tecnica e Economia delle Aziende, Genoa, 2-16126, Italy
SO Chimica e l'Industria (Milan, Italy) (2001), 83(9), 76-81
CODEN: CINMAB; ISSN: 0009-4315
PB Editrice Bias Sas
DT Journal
LA Italian
AB Perfluorocarbon compds. being developed to replace halocarbons in applications such as refrigerants, working fluids, blowing agents, and propellants are described. Alternative products based on hydrocarbons, e.g., propane, isobutane, n-pentane, isopentane, cyclopentane and on Pr bromide, are also outlined. The prospects of NH3 and CO (R 744) as alternatives to halocarbons are also discussed.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:336818 HCAPLUS
DN 134:335280

TI Fabrication of semiconductor device
IN Sato, Kiyoyuki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 2001127039 | A2 | 20010511 | JP 1999-302329 | 19991025 |

AB The title method involves forming a multilayer film of a nitride bottom layer and oxide top layer on a substrate, selectively etching the oxide top layer using a first etching gas to from an opening, and etching the nitride bottom layer via the opening using a second etching gas based on CxFy such as C3F6, C4F6, C4F8, or C5F8. Addnl., the second etching gas may contain CH2F2, CH3F, CH3Br, NH3, EtOH, MeOH, CO, or CO2. The etching selectivity is improved. The method is useful for forming contact holes.

L14 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:220720 HCAPLUS
DN 132:244990
TI Method to improve the capacity of data retention and increase the coupling ratio of source to floating gate in split-gate flash
IN Lin, Yai-Fen; Hsieh, Chia-Ta; Sung, Hung-Cheng; Yeh, Chuang-Ke; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6046086 | A | 20000404 | US 1998-100691 | 19980619 |
| US 6326660 | B1 | 20011204 | US 2000-524522 | 20000313 |
| PRAI US 1998-100691 | A3 | 19980619 | | |

AB A method is provided for forming a split-gate flash memory cell having reduced size, increased capacitive coupling and improved data retention capability. A split-gate cell is also provided with appropriate gate oxide thicknesses between the substrate and the floating gate and between the floating gate and the control gate along with an extra thin nitride layer formed judiciously over the primary gate oxide layer to overcome the problems of low data retention capacity of the floating gate and the reduced capacitive coupling between the floating gate and the source of prior art.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:617150 HCAPLUS
DN 127:271329
TI Production of semiconductor device.
IN Kadomura, Shingo
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 09237783 | A2 | 19970909 | JP 1996-43561 | 19960229 |

AB The title method involves plasma CVD of a fluorinated amorphous C insulator film using a compd. capable of forming CF and/or CF2 in a plasma. Specifically, the compd. may comprise hexafluoro-2-butyne, hexafluoro-1,3-butadiene, hexafluoropropane, or hexafluoropropylene oxide. Addnl., N2, NH3, and/or N2H4 may be used for the plasma.

L14 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:666423 HCAPLUS
DN 126:7647
TI 2H-Heptafluorobut-2-ene as a synthon for hexafluorobut-2-yne
AU Chambers, Richard D.; Roche, Alex J.
CS Department of Chemistry, University of Durham, South Road, Durham, DH1 3LE, UK
SO J. Fluorine Chem. (1996), 79(2), 139-143
CODEN: JFLCAR; ISSN: 0022-1139
PB Elsevier
DT Journal
LA English
OS CASREACT 126:7647
AB Reactions of heptafluorobut-2-ene with nucleophiles are described, in some cases giving products analogous to those previously obtained from hexafluorobut-2-yne. Depending on the conditions, hydrolysis can lead to 1,1,1,4,4,4-hexafluorobutan-2-one, or 1,1,1-trifluoroacetone. Reactions with diols, bis-phenols, ammonia and amines are also described.

L14 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:191167 HCAPLUS
DN 118:191167
TI Purification of hexafluoropropylene
IN Kawazoe, Niro; Kawasaki, Toru; Tomota, Katsuhiko
PA Asahi Glass Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 04346949 | A2 | 19921202 | JP 1991-146695 | 19910522 |

AB Hexafluoropropylene (I) contg. perfluorobutyne-2 (II) is treated with org. compds. having lone electron pairs to remove II. I contg. 2 mol% II was treated with MeOH soln. of aniline for 30 min to show 0% II.

L14 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:115639 HCAPLUS
DN 118:115639
TI Preparation and characterization of thermally stable (cyclo-SeNSeNSe)n(AsF6)2 containing the 'electron-rich aromatic' 6.pi. (cyclo-SeNSeNSe)2+ (n = 1) and 7.pi. cyclo-SeNSeNSe.bul.+ (n = 2)
AU Awere, Edward G.; Passmore, Jack; White, Peter S.
CS Dep. Chem., Univ. New Brunswick, Fredericton, NB, E3B 6E2, Can.
SO J. Chem. Soc., Dalton Trans. (1993), (2), 299-310
CODEN: JCDTBI; ISSN: 0300-9246
DT Journal
LA English

AB Cryst. thermally stable (SeNSeNSe)n(AsF6)2 contg. the electron-rich arom. 6.pi. SeNSeNSe2+ (n = 1) and 7.pi. radical cation SeNSeNSe.bul.+ (n = 2) were prepd. in high yields from reactions of Se4N4 with stoichiometric quantities of Se4(AsF6)2 (n = 1) or AsF5 (n = 1 or 2) in liq. SO2 and their x-ray crystal structures detd. The structure of SeNSeNSe(AsF6)2 consists of discrete planar SeNSeNSe2+ and AsF6- and that of (SeNSeNSe)2(AsF6) consists of 2 identical, but crystallog. different, discrete (SeNSeNSe.bul.+)2 and AsF6-. The centrosym. (SeNSeNSe.bul.+)2 dimer contains 2 planar SeNSeNSe.bul.+ radical cations weakly joined by 2 long Se...Se bonds [2 .times. 3.123(3), 2 .times. 3.149(3) .ANG.]. There are significant cation-anion interactions in both salts. The Se-Se [2.334(3) .ANG.] and Se-N bond lengths [av.: 1.74(3) (side), 1.69(3) .ANG. (top)] in SeNSeNSe2+ are shorter than their corresponding distances in the 7.pi. SeNSeNSe.bul.+ [av.: Se-Se 2.398(3); Se-N 1.76(2) (side), 1.69(2) (top) .ANG.] consistent with removal of the unpaired electron from the .pi.* singly occupied MO of the monocation. Only 1 peak, rather than the expected 2, was obsd. in the 77Se NMR spectrum of SeNSeNSe(AsF6)2 consistent with fluxional behavior in soln. The 77Se chem. shift [-70.degree., .delta.(Me2Se) = 2434, .nu.1/2 = 10 Hz] is the highest so far recorded and is consistent with the dipos. charge and electron-rich 6.pi. arom. character. The 77Se and 17N NMR [room temp. (r.t.), .delta.(MeNO2) = -67.6, .nu.1/2 = 200 Hz] and the Raman spectrum in liq. AsF3 at 10.degree. are all consistent with retention of the SeNSeNSe2+ ring structure in soln. The ESR spectrum of SeNSeNSe.bul.+ in SO2 soln. at r.t. (g = 2.043, broad) and the spectrum of powd. SeNSeNSe.bul.+ in frozen SO2 at -160.degree. were similar to but not identical with those of SeNSNSe.bul.+, SeNSNS.bul.+, and SNSNS.bul.+, indicative of a planar 7.pi. ring system.

L14 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1982:181418 HCAPLUS
DN 96:181418
TI Binuclear organoplatinum complexes as models for catalytic intermediates
AU Brown, M. P.; Fisher, J. R.; Franklin, S. J.; Puddephatt, R. J.; Thomson, M. A.
CS Donnan Lab., Univ. Liverpool, Liverpool, UK
SO Adv. Chem. Ser. (1982), 196(Catal. Aspects Met. Phosphine Complexes), 231-41
CODEN: ADCSAJ; ISSN: 0065-2393
DT Journal
LA English
AB Attempts have been made to mimic proposed steps in catalysis at a Pt metal surface using well-characterized binuclear Pt complexes. A series of such complexes, stabilized by bridging bis(diphenylphosphino)methane ligands, has been prepd. and structurally characterized. Included are diplatinum(I) complexes with Pt-Pt bonds, complexes with bridging hydride, carbonyl or methylene groups, and binuclear methylplatinum complexes. Reactions of these complexes have been studied and new binuclear oxidative addn. and reductive elimination reactions, and a new catalyst for the water gas shift reaction have been discovered.

L14 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1977:120853 HCAPLUS
DN 86:120853
TI Synthesis and reactions of tetracyclo[4.2.0.02,4.03,5]octanes
AU Smith, Leverett R.; Gream, George E.; Meinwald, Jerrold
CS Spencer T. Olin Lab., Cornell Univ., Ithaca, N. Y., USA
SO J. Org. Chem. (1977), 42(6), 927-36
CODEN: JOCEAH

DT Journal
LA English
AB Tetracyclo[4.2.0.0.2,4]oct-7-ene (I) was prepd. in 4 steps, starting with benzvalene. The adduct which formed readily by addn. of Cl2C:CO to benzvalene was dehalogenated with Ph3SnH, and the resulting ketone II (R = H) was converted to I by the reaction of its p-toluenesulfonylhydrazone with lithium 2,2,6,6-tetramethylpiperidide. Isomerization of I to cyclooctatetraene occurred thermally, photochem., and in a Ag+-catalyzed reaction. Reaction of I with N-phenyltriazolinedione yielded a hexacyclic adduct III.

L14 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1974:101755 HCAPLUS
DN 80:101755
TI Prediction of core-level binding-energy shifts from CNDO [complete neglect of differential overlap] molecular orbitals
AU Davis, D. W.; Shirley, D. A.
CS Lawrence Berkeley Lab., Univ. California, Berkeley, Calif., USA
SO J. Electron Spectrosc. Relat. Phenomena (1974), 3(2), 137-63
CODEN: JESRAW
DT Journal
LA English
AB A theory is described for calcg. core-level binding-energy shifts with potential models that employ intermediate-level MO wave functions. The relaxation-energy term in at. core-level binding energies is considered 1st. The ground-state potential model (GPM) and relaxation-potential model (RPM) are developed for calcg. core-level binding energy shifts in mols. from CNDO wave functions. Neglect of certain 2- and 3-center integrals in these models limits their accuracy when unlike mols. are compared. The models are modified by calcg. .ltbbrac.r-1.rtbbrac. integrals, to be sensitive to bond directions of p orbitals. The pp' modification, in which a subset of the neglected integrals is retained to recover invariance to coordinate transformations, is thereby necessitated. The GPM approach yields in very good agreement with expt. when comparisons are restricted to similar mols. The RPM version gives better agreement, esp. over wider classes of mols. It also provides relaxation energies VR that can be combined with ab initio orbital energies to give binding energies. Several applications of these potential models are discussed.

L15 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:256791 HCAPLUS
DN 136:287681
TI Method of manufacturing a semiconductor integrated circuit device with high aspect ratio hole or trench
IN Ikeda, Takenobu; Tadokoro, Masahiro; Izawa, Masaru; Yunogami, Takashi
PA Japan
SO U.S. Pat. Appl. Publ., 59 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 2002039843 | A1 | 20020404 | US 2001-964628 | 20010928 |
| JP 2002110647 | A2 | 20020412 | JP 2000-299854 | 20000929 |
| PRAI JP 2000-299854 | A | 20000929 | | |

AB A hole is formed on an insulating film made of Si oxide by selectively plasma-etching the insulating film with an etching gas contg. C5F8, O2, and Ar firstly under a condition in which the deposition property of a polymer layer is weak and secondly under a condition in which that of the polymer layer is strong.

L15 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:380935 HCAPLUS
DN 134:360410
TI Materials and gas chemistries for plasma processing substrates with a high degree of uniformity across the surfaces
IN Bailey, Andrew D., III; Schoepp, Alan M.; Hemker, David J.; Wilcoxson, Mark H.
PA Lam Research Corporation, USA
SO PCT Int. Appl., 54 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI WO 2001037314 | A1 | 20010525 | WO 2000-US31229 | 20001114 |
| W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM | | | | |
| RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG | | | | |
| PRAI US 1999-440794 | A | 19991115 | | |

AB A plasma processing system for processing a substrate, is disclosed. The plasma processing system includes a single chamber, substantially azimuthally sym. plasma processing chamber within which a plasma is both ignited and sustained for the processing. The plasma processing chamber has no sep. plasma generation chamber. The plasma processing chamber has an upper end and a lower end. The plasma processing chamber includes a material that does not substantially react with the reactive gas chemistries that are delivered into the plasma processing chamber. In addn., the reactant gases that are flown into the plasma processing

chamber are disclosed.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L15 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:336818 HCAPLUS
DN 134:335280
TI Fabrication of semiconductor device
IN Sato, Kiyoyuki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 2001127039 | A2 | 20010511 | JP 1999-302329 | 19991025 |

AB The title method involves forming a multilayer film of a nitride bottom layer and oxide top layer on a substrate, selectively etching the oxide top layer using a first etching gas to from an opening, and etching the nitride bottom layer via the opening using a second etching gas based on CxFy such as C3F6, C4F6, C4F8, or C5F8. Addnl., the second etching gas may contain CH2F2, CH3F, CH3Br, NH3, EtOH, MeOH, CO, or CO2. The etching selectivity is improved. The method is useful for forming contact holes.

L24 ANSWER 1 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:327871 HCAPLUS
TI Methods for cleaving facets in III-V nitrides grown on c-face sapphire substrates in laser diodes and light-emitting devices
IN Cervantes, Tanya J.; Romano, Linda T.; Kneissl, Michael A.
PA Xerox Corporation, USA
SO U.S., 21 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6379985 | B1 | 20020430 | US 2001-682181 | 20010801 |

AB Methods for cleaving semiconductor structures formed on c-face sapphire substrates are disclosed. An exemplary method includes forming .gtoreq.1 III-V nitride layer on the top c-face of a c-face sapphire substrate. A line of weakness is formed on the bottom c-face of the c-face sapphire substrate in the a-plane direction of the c-face sapphire substrate. A force is applied to the bottom c-face to cleave the c-face sapphire substrate along the line of weakness in the a-plane direction, and to form a cleaved facet along an m-plane of each III-V nitride layer. The III-V nitride layers can be included in laser diodes and other light-emitting devices.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 2 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:251922 HCAPLUS
DN 136:271784
TI Method of processing a substrate in a processing chamber in way of reduction of cycle time for processing apparatus
IN Lee, Albert; Ngai, Chris; Bencher, Christopher; Nowak, Tom
PA Applied Materials, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6365518 | B1 | 20020402 | US 2001-818361 | 20010326 |

AB A substrate with a 1st **layer** and an **oxide layer** on the substrate is placed in a processing chamber. The **oxide layer** is removed while the substrate is at a 1st temp. in the processing chamber. A 2nd layer is then formed on the 1st layer while the substrate is at a 2nd temp. in the processing chamber.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 3 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:182156 HCAPLUS
DN 136:239961
TI Metallization structure, and associated method, to improve crystallographic texture and cavity fill for CVD aluminum/PVD aluminum alloy films
IN Dixit, Girish; Konecni, Anthony
PA Texas Instruments Incorporated, USA

SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6355558 | B1 | 20020312 | US 1999-332362 | 19990610 |

AB A metalization structure, and assocd. method, for filling contact and via apertures to significantly reduce the occurrence of microvoids and provide desirable grain orientation and texture. A modified barrier structure is set forth for contact apertures, and a modified liner structure is set forth for via apertures. The metalization fill structure for contact apertures includes a 1st wetting or glue layer of refractory metal on the contact aperture, a layer of TiN on the 1st wetting layer, a 2nd wetting layer of plasma-treated refractory metal on the barrier layer, a layer of CVD Al on the 2nd wetting refractory metal layer, and a PVD Al alloy to fill the contact aperture. The fill structure for via apertures includes an initial plasma-treated refractory metal liner deposited on the via aperture. A CVD Al liner is positioned on the initial refractory metal liner. A PVD Al alloy layer is positioned on the CVD Al liner to fill the via aperture.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 4 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:84583 HCAPLUS
DN 136:143901
TI Plasma process for organic residue removal from copper
IN Smith, Patricia B.; Rotondaro, Antonio L. P.
PA Texas Instruments Incorporated, USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6342446 | B1 | 20020129 | US 1999-407418 | 19990929 |
| PRAI US 1998-103455P | P | 19981006 | | |

AB The invention pertains to semiconductor device fabrication and processing and more specifically to post metal pattern and **etch** cleanup processing. An embodiment of the instant invention is a method of fabricating an electronic device formed on a semiconductor wafer, the method comprising the steps of: forming a conductive structure over the semiconductor substrate, the conductive structure comprised of an O-sensitive conductor and having an exposed surface; oxidizing a portion of the conductive structure; and subjecting the conductive structure to a plasma which incorporates H2 or D2.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 5 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:66756 HCAPLUS
DN 136:127547
TI Silicon nitride as antireflective coating
IN Feng, Joe; Patel, Anjana M.; Shek, Mei Yee; Huang, Judy H.; Ngai, Christopher S.
PA Applied Materials, Inc., USA

SO Eur. Pat. Appl., 12 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI EP 1174911 | A2 | 20020123 | EP 2001-113399 | 20010601 |
| R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO | | | | |
| PRAI US 2000-587355 | A | 20000605 | | |

AB A method of forming an integrated circuit using a Si nitride antireflective coating (ARC) is disclosed. The Si nitride layer is formed by reacting a Si-contg. compd. with a N-contg. compd. The Si nitride layer is compatible with integrated circuit fabrication processes. In 1 integrated circuit fabrication process, the Si nitride ARC is used as a hard mask. In another integrated circuit fabrication process, the Si nitride ARC is incorporated into a damascene structure.

L24 ANSWER 6 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:863472 HCAPLUS
DN 135:379562
TI Borderless self-aligned, dual damascene contact formation
IN Shih, Cheng-yeh; Lee, Yu-hua; Wu, James
PA Taiwan Semiconductor for Manufacturing Company, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6323118 | B1 | 20011127 | US 1998-114129 | 19980713 |

AB A method is disclosed for forming self-aligned, borderless contact and vias together and simultaneously with relaxed photolithog. alignment tolerances using a modified dual damascene process having two **etch**-stop layers. A 1st **etch**-stop layer is formed over a 1st **dielec. layer**. A 2nd **dielec. layer** and a 2nd **etch**-stop layer are next formed sequentially over the 1st **etch**-stop layer. Contact/via hole pattern is **etched** into the 1st **etch**-stop layer using a 1st photoresist layer. A 2nd photoresist layer, patterned with metal line trench pattern, is formed over the contact/via patterned 1st **etch**-stop layer. The contact/via hole openings are **etched** into the 1st **dielec. layer** until the 2nd **etch**-stop layer is reached. Then, both the 1st and 2nd **etch**-stop layers are **etched** through the openings. The openings in the 1st and 2nd **etch**-stop layers are both extended by **etching** the 2nd and 1st **dielec. layers**, resp., until the former opening reaches the 2nd **etch**-stop layer, and the latter reaches the underlying substructure of devices within the semiconductor substrate. Thus, a combination of contact via interconnects, without borders, and self-aligned with respect to metal lines with relaxed photolithog. tolerances is formed together and simultaneously using a modified dual damascene process having two **etch**-stop layers.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 7 OF 40 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:821769 HCAPLUS
DN 135:338005
TI Improved manufacturing method for capacitors in high density memory device
IN Sung, Jian-Mai
PA Vanguard International Semiconductor Corporation, Taiwan
SO Taiwan, 21 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| TW 381339 | B | 20000201 | TW 1995-84111548 | 19951101 |

AB An improved capacitor fabrication technique is presented for stack dynamic random access memory. A dielec. spacer structure is formed by film deposition and plasma **etching** techniques to increase the area of storage node, the capacitance of Stack DRAM capacitors and the integration d. of memory devices of high value Stack DRAM.

L24 ANSWER 8 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:792285 HCAPLUS
DN 135:326136
TI Design and fabrication of a split-gate flash memory cell
IN Sung, Hung-cheng; Kuo, Di-son; Yeh, Chuang-ke; Hsieh, Chia-ta; Lin, Yai-fen; Chu, Wen-ting
PA Taiwan Semiconductor Manufacturing Co., Taiwan
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6309928 | B1 | 20011030 | US 1998-208913 | 19981210 |
| US 2002027241 | A1 | 20020307 | US 2001-920601 | 20010802 |
| PRAI US 1998-208913 | A3 | 19981210 | | |

AB A method of forming a 1st polysilicon gate tip (poly-tip) for enhanced F-N tunneling in split-gate flash memory cells is disclosed. The poly-tip is formed in the absence of using a thick polysilicon layer as the floating gate. This is made possible by forming an **oxide layer** over the poly-gate and oxidizing the sidewalls of the polygate. Because the starting thickness of polysilicon of the floating gate is relatively thin, the resulting gate beak, or poly-tip, is also necessarily thin and sharp. This method, therefore, circumvents the problem of oxide thinning encountered in scaling down devices of the ultra large scale integration technol. and the fast programmability and erasure performance of EEPROMs is improved.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 9 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:614311 HCAPLUS
DN 135:188909
TI Oxygen-free, dry plasma process for polymer removal in fabricating an electronic device
IN Smith, Patricia B.
PA Texas Instruments Incorporated, USA
SO U.S., 9 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6277733 | B1 | 20010821 | US 1999-408022 | 19990929 |
| PRAI US 1998-103047P | P | 19981005 | | |

AB An embodiment of the instant invention is a method of fabricating an electronic device formed on a semiconductor wafer, the method comprising the steps of: forming a conductive structure over the substrate, the conductive structure comprised of an O-sensitive conductor; forming a **layer** of **dielec**. material over the conductive structure; forming a photoresist layer over the **layer** of the **dielec**. material; patterning the **layer** of the **dielec**. material; removing the photoresist layer after patterning the **layer** of the **dielec**. material; and subjecting the semiconductor wafer to a plasma which incorporates the combination of H or D and a F-contg. mixt. which is comprised of a gas selected from the group consisting of: CF4, C2F6, CHF3, CFH3 and other F-contg. hydrocarbon.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 10 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:614305 HCAPLUS
DN 135:161177
TI Method to reduce gate oxide damage by using a multi-step **etch** process with a predictable premature endpoint system
IN Chhagan, Vijaikumar; Pradeep, Yelehanka R.; Tjoa, Tjin Tjin
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6277716 | B1 | 20010821 | US 1999-425908 | 19991025 |

AB A method of fabricating a gate stack having an endpoint detect layer and a multi-step **etch** process to prevent damage to a gate **dielec**. **layer**. The special endpoint detect layer emits an endpoint signal that allows the **etch** chem. to be changed to a more selective polysilicon to oxide ratio to prevent damage to the gate **oxide layer**. The invention begins by forming a gate **dielec**. **layer** over a substrate. The authors then form an endpoint detect **layer** over the gate **dielec**. **layer**. A gate stack is formed over the bottom Si layer. Then a mask is formed over the gate stack. The mask defines a gate electrode. The authors **etch** the gate stack and the endpoint detect layer using a multi-step **etch** comprising at least 3 steps. In a main **etch** step, the gate stack and the endpoint detect layer are **etched** using a 1st **etch** chem. Upon an endpoint detection signal generated by **etching** the gate stack, the 1st **etch** step is stopped. In an endpoint detect layer **etch** step, the gate stack layer and the endpoint detect layer are **etched** using a 2nd **etch** chem. The endpoint **etch** step is stopped when an endpoint detect signal changes upon reaching the gate **dielec**. **layer**. The 2nd **etch** chem. has a higher selectivity from the gate **dielec**. **layer** to the gate stack layer and endpoint detect layer than the 1st **etch**

chem. In an overetch step, using a 3rd **etch** chem. with a higher selectivity than the 2nd **etch** chem., the authors **etch** the endpoint detect layer without damaging the gate **dielec. layer**.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 11 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:366698 HCAPLUS
DN 134:360252
TI Method for **etching** a trench having rounded top and bottom corners in a silicon substrate
IN Mui, David; Podlesnik, Dragan; Liu, Wei; Lee, Gene; Kim, Nam-hun; Chinn, Jeff
PA Applied Materials, Inc., USA
SO U.S., 21 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6235643 | B1 | 20010522 | US 1999-371966 | 19990810 |
| US 6180533 | B1 | 20010130 | US 2000-545700 | 20000407 |
| PRAI US 1999-371966 | A2 | 19990810 | | |

AB The present invention provides straight forward methods for plasma **etching** a trench having rounded top corners, or rounded bottom corners, or both in a Si substrate. A 1st method for creating a rounded top corner on the **etched** Si trench comprises **etching** both an overlying Si **oxide layer** and an upper portion of the Si substrate during a break-through step which immediately precedes the step in which the Si trench is **etched**. The plasma feed gas for the break-through step comprises C and F. In this method, the photoresist layer used to pattern the **etch** stack is preferably not removed prior to the break-through **etching** step. Subsequent to the break-through step, a trench is **etched** to a desired depth in the Si substrate using a different plasma feed gas compn. A 2nd method for creating a rounded top corner on the **etched** Si trench comprises formation of a built-up extension on the sidewall of an overlying patterned Si nitride hard mask during **etch** (break-through) of a Si **oxide** adhesion **layer** which lies between the hard mask and a silicon substrate. The built-up extension upon the Si nitride sidewall acts as a sacrificial masking material during **etch** of the Si trench, delaying **etching** of the Si at the outer edges of the top of the trench. This permits completion of trench **etching** with delayed **etching** of the top corner of the trench and provides a more gentle rounding (increased radius) at the top corners of the trench. During the **etching** of the Si trench to its final dimensions, it is desirable to round the bottom corners of the finished Si trench. A more rounded bottom trench corner was obtained using a two-step Si **etch** process where the 2nd step of the process is carried out at a higher process chamber pressure than the 1st step.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 12 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:338170 HCAPLUS
DN 134:335430

TI Method for detecting an end point for an oxygen free plasma process
IN Han, Quigyan; Sakthivel, Palani; Ruffin, Ricky; Cardoso, Andre Gil
PA Axcelis Technologies, Inc., USA
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI EP 1098189 | A2 | 20010509 | EP 2000-309763 | 20001103 |
| EP 1098189 | A3 | 20020417 | | |
| R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO | | | | |
| JP 2001189305 | A2 | 20010710 | JP 2000-337593 | 20001106 |
| PRAI US 1999-434617 | A | 19991105 | | |

AB A method for detg. an endpoint for an O free plasma stripping process for use in semiconductor wafer processing. The method comprises exciting a gas compn. contg. a N gas and a reactive gas to form the O free plasma. The O free plasma reacts with a substrate 88 having a photoresist and/or residues thereon to produce emitted light signals corresponding to an O free reaction product. The endpoint is detd. by optically measuring a primary emission signal of the O free reaction product at a wavelength of .apprx.387nm. The endpoint is detd. when the plasma no longer reacts with the photoresist and/or residues on the substrate to produce the emitted light at .apprx.387nm, an indication that the photoresist and/or residues have been removed from the wafer. Secondary emission signals of the O free reaction product at .apprx.358nm and 431 nm can also be monitored for detg. the endpoint.

L24 ANSWER 13 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:224383 HCAPLUS
DN 134:260190
TI Photoresist ashing process for organic and inorganic polymer dielectric materials
IN Dunne, Jude; Kennedy, Joseph; Luo, Leroy Laizhong; Howell, Diane Cecile; Kuhl, Nicole Eliette Charlotte
PA Alliedsignal Inc., USA; Mattson Technologies
SO U.S., 23 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6207583 | B1 | 20010327 | US 1999-390143 | 19990903 |
| PRAI US 1998-99246P | P | 19980904 | | |

AB A process for removal of photoresist present on a polymer dielec. on a semiconductor substrate and for removal of photoresist residues on the inside walls of microvias formed in the **dielec. layer**. The process is conducted by generating a plasma in a plasma generator from a gas comprising one or more F compd. contg. **etchant** gases and **etching** the substrate having a **dielec. layer** thereon, and a photoresist **layer** on the **dielec. layer** and on the inside walls of microvias formed in the **dielec. layer**. The **etching** is conducted at a temp. of from .apprx.0.degree.. to .apprx.90.degree.. and at a pressure of from .apprx.10 torr or less, to thereby remove the photoresist present on the **dielec. layer** and on the inside walls of the

microvias.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 14 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:195156 HCAPLUS
DN 134:216056
TI Post-spacer **etch** surface treatment for improved silicide formation in MOS transistor fabrication
IN Chan, Simon S.; Ngo, Minh Van; Besser, Paul R.; Hui, Angela T.
PA Advanced Micro Devices, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6204136 | B1 | 20010320 | US 1999-386466 | 19990831 |

AB Sub-micron dimensioned, ultra-shallow junction MOS and/or CMOS transistor devices having reduced or minimal junction leakage are formed by a salicide process wherein carbonaceous residue on Si substrate surfaces resulting from reactive plasma **etching** for sidewall spacer formation is removed prior to salicide processing. Embodiments include removing carbonaceous residues by performing a H ion plasma treatment.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 15 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:91464 HCAPLUS
DN 134:140416
TI Method to eliminate silicide cracking for NAND type flash memory devices by implanting a polish rate improver into the second polysilicon layer and polishing it
IN Chi, David; Chang, Kent Kuohua; He, Yuesong
PA Advanced Micro Devices, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6184084 | B1 | 20010206 | US 1999-263701 | 19990305 |

AB A flash memory cell having improved reliability is obtained by providing an improved tungsten silicide conductive layer. A tunnel oxide is formed on a substrate. A first polysilicon layer is formed over the tunnel oxide, followed by an **insulating layer** formation over the first polysilicon layer. A second polysilicon layer is formed over the **insulating layer** by depositing a second polysilicon layer having a first thickness, and then using chem. mech. polishing to form a second polysilicon layer having a second thickness, in which the second thickness is at least .apprx.25% less than the first thickness. A tungsten silicide layer is formed over the second polysilicon layer by CVD using WF6 and SiH4. The first polysilicon layer, the second polysilicon **layer**, the **insulating layer**, and the W silicide layer are **etched**, thereby defining .gtoreq.1 stacked gate structure. A source region and a drain region in the substrate are formed, thereby forming .gtoreq.1 memory cell.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 16 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:45125 HCAPLUS
DN 134:94392
TI Optimal process flow of fabricating nitride spacer without inter-poly oxide damage in split gate flash memory
IN Hsieh, Chia-ta; Lin, Yai-fen; Sung, Hung-cheng; Yeh, Jack; Kuo, Di-son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6174772 | B1 | 20010116 | US 1999-347548 | 19990706 |

AB A method is disclosed to form a split-gate flash memory cell having nitride spacers formed on a pad oxide and prior the forming of an inter-poly **oxide layer** there over. In this manner, any damage that would normally occur to the inter-poly oxide during the **etching** of the nitride spacers subsequent to the forming of the inter-poly oxide is avoided. Consequently, the variation in the thickness of the inter-poly oxide due to the unpredictable damage to the underlying spacers is also avoided by reversing the order in which the spacers and the inter-poly oxide are formed, including the forming of the pad oxide 1st. As a result, variation in the erase speed of the inter-gate flash memory cell is prevented, both for cells fabricated on the same wafer as well as on different wafers on same or different prodn. lines.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 17 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:822801 HCAPLUS
DN 133:358246
TI High-speed TFT and method for its fabrication
IN Yamazaki, Shunpei; Arai, Yasuyuki
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 49 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| EP 1054452 | A2 | 20001122 | EP 2000-110387 | 20000515 |
| R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO | | | | |
| JP 2001053285 | A2 | 20010223 | JP 2000-142027 | 20000515 |
| PRAI JP 1999-171485 | A | 19990515 | | |
| JP 1999-152902 | A | 19990531 | | |

AB To fabricate a cryst. semiconductor film with controlled locations and sizes of the crystal grains, and to use the cryst. semiconductor film in the channel-forming region of a TFT to realize a high-speed operable TFT. A translucent **insulating** thermal conductive **layer** 2 is provided in close contact with the main surface of a substrate 1, and an insular or striped 1st **insulating layer** 3 is formed in selected regions on the thermal conductive layer. A 2nd

**insulating layer** 4 and semiconductor film 5 are laminated there over. The semiconductor film 5 is 1st formed with an amorphous semiconductor film, and then crystd. by laser annealing. The 1st **insulating layer** 3 has the function of controlling the rate of heat flow to the thermal conductive layer 2, and the temp. distribution difference on the substrate 1 was used to form a single-crystal semiconductor **film** on the 1st **insulating layer** 3.

L24 ANSWER 18 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:802354 HCAPLUS
DN 133:328536
TI Method for manufacturing a thin oxide for use in semiconductor integrated circuits
IN Wu, Wei Edwin; Tseng, Hsing-Huang; Crabtree, Phillip Earl; Lii, Yeong-Jyh Tom
PA Motorola Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6146948 | A | 20001114 | US 1997-868331 | 19970603 |

AB A method for forming a gate dielec. having different thickness begins by providing a substrate. A sacrificial oxide is formed overlying the substrate. A 1st portion of the sacrificial oxide is exposed to a C-contg. plasma environment. This C-contg. plasma environment forms a C-contg. layer within the region. After forming this region, a wet **etch** chem. is used to remove remaining portions of the sacrificial **oxide** without forming a **layer** in the region. Furnace oxidn. is then used to form regions in which the growth of region has been retarded by the presence of the region. Therefore, the regions are differing in thickness and can be used to make different transistors having different current gains.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 19 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:680376 HCAPLUS
DN 133:246184
TI Hydrogen removal method of making intermetal hydrogen silsesquioxane **dielectric layers** having a low **dielectric** constant and reduced numbers of voids for semiconductor devices
IN Ko, Ho; Kim, Tae-Ryong; Kim, Chung-Howan; Kim, Dong-Yun; Song, JongHeui
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6124216 | A | 20000926 | US 1999-393185 | 19990910 |
| KR 2000056081 | A | 20000915 | KR 1999-5109 | 19990212 |
| PRAI KR 1999-5109 | A | 19990212 | | |

AB A method of forming a low-k **dielec. insulating layer** includes forming the **dielec. insulating**

**layer** and then removing H bonds in the **dielec.** **insulating layer**. The **dielec. layer** as formed is preferably a HSQ film which contains the structure Si--O--H. H is removed from the **dielec. layer** by either: a heat treatment in plasma, an ozone redn. process, an ion implantation process, or electron beam bombardment.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 20 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:509037 HCAPLUS
DN 133:98186
TI Method for forming trench isolation in semiconductor device
IN Koo, Bon-Young; Hong, Gyung-Hoon; Bae, Dae-Hoon
PA Samsung Electronics Co., Ltd., S. Korea
SO Faming Zhuanli Shenqing Gongkai Shuomingshu, 14 pp.
CODEN: CNXXEV
DT Patent
LA Chinese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | CN 1233851 | A | 19991103 | CN 1999-106000 | 19990427 |
| PRAI | KR 1998-14921 | A | 19980427 | | |

AB The method comprises forming trench with round bottom edge in semiconductor substrate by **etching**, forming thermal oxidn. layer in the trench at .gtoreq. 1000.degree., forming oxidn. barrier **insulating layer**, filling the trench with insulating material, and annealing the insulating material in NH3 or N2 for nitridation. The trench has depth .apprx. 2500 .ANG., width .apprx. 2100 .ANG., and thermal oxidn. layer thickness .ltoreq. .apprx. 240 .ANG.. The **etching** process comprises vertical **etching** of semiconductor substrate using CF4 and round **etching** of trench hemline using a mixed gas of Cl2, HBr, He, and O2. A method for manufg. semiconductor device comprises forming trench in semiconductor substrate, forming thermal oxidn. layer in the trench, forming oxidn. barrier **layer**, filling **insulation** material in the trench, planarization of the **insulation layer** to form trench **insulation**, forming transistor on the semiconductor substrate, (consisting of gate **oxide layer**, gate electrode, the first Si3N4 mask, side-wall **insulation layer** formed from the first CVD **oxide layer** and the second Si3N4 layer, and source/drain electrode), and forming the second CVD **oxide layer**.

L24 ANSWER 21 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:420893 HCAPLUS
DN 133:52161
TI Fabrication of semiconductor memory devices from ferroelectric films
IN Tamura, Akiyoshi
PA Matsushita Electronics Corporation, Japan
SO Eur. Pat. Appl., 40 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 1011149 | A2 | 20000621 | EP 1999-124901 | 19991214 |

EP 1011149 A3 20000927
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO
JP 2000183295 A2 20000630 JP 1998-357504 19981216
US 6380573 B1 20020430 US 1999-460062 19991214
PRAI JP 1998-357504 A 19981216
AB A semiconductor memory device includes a semiconductor substrate having a channel therein; a gate **insulating layer** formed of a ferroelec. material provided on the semiconductor substrate; and a gate electrode provided on the gate **insulating layer**.. The ferroelec. material includes nitrogen and at least one element selected from the group consisting of Mg, Sr, Ba and Ca.

L24 ANSWER 22 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:381698 HCAPLUS
DN 132:355744
TI Method of filling contact holes and wiring grooves of a semiconductor device
IN Wada, Junichi; Sakata, Atsuko; Katata, Tomio; Usui, Takamasa; Hasunuma, Masahiko; Shibata, Hideki; Kaneko, Hisashi; Hayasaka, Nobuo; Okumura, Katsuya
PA Kabushiki Kaisha Toshiba, Japan
SO U.S., 106 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6071810 | A | 20000606 | US 1997-997328 | 19971223 |
| JP 10189495 | A2 | 19980721 | JP 1996-344264 | 19961224 |
| JP 10242279 | A2 | 19980911 | JP 1997-350382 | 19971219 |

PRAI JP 1996-344264 A 19961224
JP 1996-344265 A 19961224
JP 1997-350382 A 19971219
AB A method of manufg. semiconductor device which comprises the steps of forming an **insulating film** on an Si substrate provided with a wiring layer, forming a contact hole connected to the wiring layer and a wiring groove in the **insulating film**, filling the contact hole with an Si film, successively forming an Al film and a Ti film all over the substrate,. Performing a heat treatment thereby to substitute the Al film for the Ti film, and to allow the Si film to be absorbed by the Ti film, whereby filling the contact hole and wiring groove with the Al film, and removing a Ti/Ti silicide which is consisting of Ti silicide formed through the absorption of the Si film by the Ti film and a superfluous Ti, whereby filling the contact hole with an Al plug and filling the wiring groove with an Al wiring.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 23 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:201079 HCAPLUS
DN 132:230692
TI Robust dual damascene process for preparing interconnects in semiconductor substrate of ultra-large-scale integrated circuits
IN Lin, Cheng-tung; Lee, Yu-hua; Huang, Jenn Ming; Wu, Cheng-ming
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| US 6042999 | A | 20000328 | US 1998-73952 | 19980507 |

AB A robust dual damascene process is disclosed where the substructure in a substrate is protected from damage caused by multiple **etchings** required in a damascene process by filling a contact or via hole opening with a protective material prior to the forming of the conductive line opening of the damascene structure having an **etch**-stop layer sepg. a lower and an upper **dielec. layer**. In the 1st embodiment, the protective material is partially removed from the hole opening reaching the substructure prior to the forming of the upper conductive line opening by **etching**. In the 2nd embodiment, the protective material in the hole is removed at the same time the upper conductive line opening is formed by **etching**. In a 3rd embodiment, the disclosed process is applied without the need of an **etch**-stop layer for the dual damascene process of this invention.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 24 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:753456 HCAPLUS
DN 131:359107
TI Substrate treatment in semiconductor device fabrication
IN Merry, Walter Richardson
PA Applied Materials, Inc., USA
SO PCT Int. Appl., 36 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 2

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| WO 9960620 | A1 | 19991125 | WO 1999-US9392 | 19990429 |
| W: JP | | | | |
| PRAI US 1998-79845 | | 19980515 | | |

AB In a process for treating a semiconductor substrate, polymeric **etchant** deposits, Si lattice damage, and native SiO2 layers are removed in sequential process steps. The polymeric **etchant** deposits are removed using an activated cleaning gas comprising inorg. fluorinated gas and O. Si lattice damage is **etched** using an activated **etching** gas. Thereafter, an activated reducing gas comprising a H-contg. gas is used to reduce the native SiO2 layer, on the substrate, to a Si layer. Subsequently, a metal layer is deposited on the substrate and the substrate is annealed to form a metal silicide layer. Removal of the polymeric **etchant** deposits, the Si lattice damage, and the native Si **oxide layer** increases the cond. of the metal silicide-Si-contg. substrate interface.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 25 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:234095 HCAPLUS
DN 130:260787
TI Cleaning of contamination from electron-emissive elements
IN Knall, N. Johan; Porter, John D.; Stanners, Colin D.; Spindt, Christopher J.; Bascom, Victoria A.

PA Candescent Technologies Corporation, USA
SO PCT Int. Appl., 38 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI WO 9917323 | A2 | 19990408 | WO 1998-US18509 | 19980922 |
| W: JP, KR | | | | |
| RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE | | | | |
| EP 1021818 | A2 | 20000726 | EP 1998-950613 | 19980922 |
| R: DE, FR, GB, NL, IE | | | | |

PRAI US 1997-940873 A 19970930
WO 1998-US18509 W 19980922

AB Multiple procedures are presented for removing contaminant material from electron-emissive elements of an electron-emitting device. One procedure involves converting the contaminant material into gaseous products, typically by operating the electron-emissive elements, that move away from the electron-emissive elements. Another procedure entails converting the contaminant material into further material and removing the further material. An addnl. procedure involves forming surface coatings over the electron-emissive elements. The contaminant material is then removed directly from the surface coatings or by removing at least part of each surface coating.

L24 ANSWER 26 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:782162 HCAPLUS
DN 130:46345
TI Manufacture of silicon nitride **oxide** gate-**insulating film** for semiconductor integrated circuit
IN Saito, Hiroshi; Mouri, Isamu
PA Central Glass Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 10321847 | A2 | 19981204 | JP 1997-130600 | 19970521 |

AB The **insulating film** is manufd. by plasmaless or plasma **etching** a Si nitride film with a F compd. gas without damages of a Si **oxide film** and nitriding with a N compd. The film may be manufd. by removing a Si nitride **film** on a Si **oxide film** with a mixed gas contg. a F compd. and a N compd. and nitriding the **oxide film** simultaneously. The film showed good elec. properties and high barrier property to impurities.

L24 ANSWER 27 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:62315 HCAPLUS
DN 128:96550
TI Fabrication of semiconductor device, especially contact hole formation
IN Yamane, Tetsuya
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF

DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 10012734 | A2 | 19980116 | JP 1996-178463 | 19960619 |

AB The invention relates to a process for making a semiconductor device, wherein a contact hole is formed by dry **etching** of interlayer **insulation film** in a gas mixt. contg. a halogen gas and a N-contg. gas for uniform deposition of a protective film in the contact hole during the **etching** process, thereby improving the shape of the contact hole.

L24 ANSWER 28 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:550911 HCAPLUS
DN 125:183480
TI Manufacture of semiconductor device including capacitor
IN Tsunoda, Katsumi; Hirai, Masahiko
PA Asahi Chemical Ind, Japan
SO Jpn. Kokai Tokkyo Koho, 17 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 08181102 | A2 | 19960712 | JP 1994-322445 | 19941226 |

AB The device, with a capacitor comprising an under electrode, an **insulating film**, and an upper electrode formed on a substrate, is manufd. by leveling the surface of the under electrode on a field-**oxide film** by an isotropically chem.-dry **etching**, and chem.-washing it with no damage to the surface flatness. The under electrode may be Si, and the chem.-washing may use an aq. soln. of NH3-H2O2 or HF. The under electrode may be metal silicide film and the chem. washing may use an aq. soln. of NH3-H2O2, HCl-H2O2, or CH3CO2H-NH3. By the leveling and washing, electrodes in the capacitor have uniform effective-surface areas, showing improved voltage resistance and precision.

L24 ANSWER 29 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:271360 HCAPLUS
DN 124:328036
TI Semiconductor laser and its manufacture
IN Adachi, Hideto; Fukuhisa, Tosha; Kidoguchi, Isao; Oonaka, Seiji
PA Matsushita Electric Ind Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 08046291 | A2 | 19960216 | JP 1994-183336 | 19940804 |
| JP 3246207 | B2 | 20020115 | | |

AB The manuf. comprises these steps; (1) forming a 1st cond.-type optical reflector (A) of a semiconductor multilayer on a substrate, (2) laminating a 1st **insulating film** (B) on it, (3) removing a part of B to expose the surface of A, (4) growing an active layer (C) of a semiconductor crystal selectively on the exposed part of A, and (5)

laminating a 2nd cond.-type optical reflector (D) of a semiconductor multilayer on them. The A and D may comprise AlGaInN-type multilayers of different compn., and C may contain a 3rd AlGaInN-type multilayer of another compn. The C may comprise an InzGa1-zN (0.ltoreq. z .ltoreq.1) quantum-well layer and an AlxGa1-xN (0.ltoreq. x .ltoreq.1) spacer layer.

L24 ANSWER 30 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:245906 HCAPLUS
DN 124:276128
TI Semiconductor device with an amorphous carbon layer and its fabrication
IN Endo, Kazuhiko
PA Nec Corporation, Japan
SO Eur. Pat. Appl., 38 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 701283 | A2 | 19960313 | EP 1995-114253 | 19950911 |
| | EP 701283 | A3 | 19961113 | | |
| | R: DE, FR, GB, NL | | | | |
| | JP 08083842 | A2 | 19960326 | JP 1994-217470 | 19940912 |
| | JP 2748864 | B2 | 19980513 | | |
| | JP 10116908 | A2 | 19980506 | JP 1997-296721 | 19940912 |
| | JP 08222557 | A2 | 19960830 | JP 1995-21429 | 19950209 |
| | JP 2751851 | B2 | 19980518 | | |
| | JP 08236517 | A2 | 19960913 | JP 1995-35023 | 19950223 |
| | JP 2748879 | B2 | 19980513 | | |
| | JP 08264648 | A2 | 19961011 | JP 1995-64066 | 19950323 |
| | JP 2845160 | B2 | 19990113 | | |
| | CA 2157257 | AA | 19960313 | CA 1995-2157257 | 19950830 |
| | US 5698901 | A | 19971216 | US 1995-526902 | 19950912 |
| | US 6033979 | A | 20000307 | US 1997-782573 | 19970110 |
| | JP 10261716 | A2 | 19980929 | JP 1998-59511 | 19980311 |
| | JP 2956682 | B2 | 19991004 | | |
| PRAI | JP 1994-217470 | | 19940912 | | |
| | JP 1995-21429 | | 19950209 | | |
| | JP 1995-35023 | | 19950223 | | |
| | JP 1995-64066 | | 19950323 | | |
| | US 1995-526902 | | 19950912 | | |

AB The invention provides a semiconductor device in which the interlayer **dielec. layers** are amorphous C. The amorphous C film may include F. The fabrication of this device includes plasma-enhanced CVD (PCVD) using a gas mixt. including (a) CF4, C2F6, C3F8, C4F8, and/or CHF3, and (b) N2, NO, NO2, NH3, and/or NF3. The method provides amorphous C films having superior heat resistance and **etching** characteristics. By using amorphous C interlayer **dielec. layers**, the semiconductor device can operate at higher speed.

L24 ANSWER 31 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:465436 HCAPLUS
DN 109:65436
TI Method for depositing interlayer **insulator films** in fabrication of integrated circuits
IN Yano, Kosaku; Tanimura, Shoichi; Fujita, Tsutomu; Kakiuchi, Takao; Yamamoto, Hiroshi
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 62291929 | A2 | 19871218 | JP 1986-136517 | 19860612 |

AB In chem. vapor deposition (CVD) of an **insulator film** on a substrate having a metal pattern using a gas mixt. of SiH4 or Si2H6 with O2, N2O, NO, N2, or NH3 activated by high-frequency a.c., a Hg lamp, or laser, the gas mixt. contains a gas which can **etch** the metal. The method is useful for forming interlayer **insulator films** in fabrication of highly integrated circuits. A semiconductor substrate having a SiO2 film and an Al electrode pattern was coated with a SiO2 layer with excellent step-coverage by plasma CVD using a SiH4-N2O gas contg. CCl4, and then coated with a 2nd Al electrode pattern. A disconnection-free circuit was obtained.

L24 ANSWER 32 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:415770 HCAPLUS
DN 109:15770
TI Manufacture of semiconductor device with low leakage current and good noise property
IN Matsumoto, Shigenori; Hiroshima, Yoshimitsu
PA Matsushita Electronics Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 63028040 | A2 | 19880205 | JP 1986-172078 | 19860722 |

AB The title manuf. comprises formation of a substance contg. 1-50% H, heating at 300-500.degree., and removal of the H-contg. substance. A Si3N4 film was grown on the surface of a phosphate silicate glass protective **insulating film** on a SiO2 film by plasma chem. vapor deposition using SiH4 and NH3, heated at 400.degree. under 10% H-contg. N, removed by plasma **etching** using CF4, and then heated at 400.degree. under H-contg. N gas to give the title device.

L24 ANSWER 33 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:177695 HCAPLUS
DN 102:177695
TI Silicon nitride insulation of integrated-circuit wirings
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 59195846 | A2 | 19841107 | JP 1983-71592 | 19830420 |

AB Si3N4 smooth-surfaced insulation of the metal wirings of integrated circuits is obtained by 1st depositing Si3N4 on the wiring, lightly plasma **etching**, recoating with Si3N4, lightly plasma **etching**, and recoating.

L24 ANSWER 34 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:104528 HCAPLUS
DN 102:104528
TI Through-hole contacts
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 59169151 | A2 | 19840925 | JP 1983-43099 | 19830317 |
| JP 05063940 | B4 | 19930913 | | |

AB Through-hole contacts without disconnections are prepd. by coating SiO2 on Si, forming an Al wiring pattern, coating with SiO2, coating with Si3N4, over coating with SiO2, masking, reactive-ion **etching** to expose the Si3N4, **etching** the Si3N4, removing the resist, and depositing aluminum.

L24 ANSWER 35 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:130915 HCAPLUS
DN 100:130915
TI Insulation of semiconductor wiring
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 58197822 | A2 | 19831117 | JP 1982-79961 | 19820514 |

AB Interlayer insulation of Al wirings on semiconductor devices is achieved without disconnections by depositing a thin Si3N4 film over the 1st Al layer by a combined discharge and reactive sputter **etching** in a gas contg. SiH4, N2, NH3, and a sputter **etchant** such as CF4 to form smooth steps, and depositing the 2nd Al film.

L24 ANSWER 36 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:113323 HCAPLUS
DN 100:113323
TI Semiconductor-device wiring
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 58188141 | A2 | 19831102 | JP 1982-73153 | 19820427 |

AB Highly reliable high-speed semiconductor devices are fabricated by reducing the defective withstand voltage and parasitic capacitance between wiring layers by using .gtoreq.2 **insulator layers** with the 1st deposited in a glow discharge and the 2nd by vapor-phase methods to prevent hillock formation. Thus, a SiO2 layer was formed on Si, a hole was **etched** in the SiO2 down to the Si, an Al layer was deposited, a Si3N4 layer was deposited from a glow discharge in SiH4 and

NH3 at 200-300.degree., a SiO2 film was vapor deposited from a mixt. of SiH4 and O2 at 400-500.degree., the SiO2 film was pattern **etched** with HF, the revealed Si3N4 was **etched** with a CF4 plasma, and a 2nd Al wiring layer was deposited.

L24 ANSWER 37 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:78360 HCAPLUS
DN 100:78360
TI Wiring layers for semiconductor devices
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 58169938 | A2 | 19831006 | JP 1982-51407 | 19820331 |

AB Wiring layers without disconnections at the through holes are fabricated by preventing groove formation in the windows by using a fast **etching layer** between the interlayer **insulator** and the 1st wiring layer. Thus, a SiO2-coated Si substrate was 1st coated with Al and then with Si3N4, reactive-ion **etching** was done with a CF4-CCl4 mixt. through a resist pattern, this resist was ashed, a SiO2 film was deposited from a SiH4-O2 mixt., the SiO2 was pattern **etched** with a CF4-H2 mixt. until it and the Al layer were at the same levels, the resist was ashed, and Al wires were added.

L24 ANSWER 38 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1983:604061 HCAPLUS
DN 99:204061
TI Thin film
PA Nippondenso Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 58128727 | A2 | 19830801 | JP 1982-11213 | 19820127 |

AB A method for plasma chem.-vapor deposition of a thin film involves the following steps: (1) forming a 1st thin film on a substrate using a reactive gas; (2) plasma **etching** the 1st film for a certain period of time; and (3) forming a 2nd thin film having the same compn. as that of the 1st film over the remaining 1st film. The undesired deposits on the 1st film are removed and the 2nd film having smooth surfaces is prepd. The process is useful for the prepn. of a passivation film for a semiconductor device.

L24 ANSWER 39 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1983:585912 HCAPLUS
DN 99:185912
TI Semiconductor devices with electrically stable **insulator films**
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 58093235 | A2 | 19830602 | JP 1981-190609 | 19811130 |

AB The elec. stability of SiO2 **insulator films** is greatly increased by dry **etching** it in a F plasma or an **etchant** contg. HF after it has been reactive-ion **etched** with CF4 and H2 during device fabrication. Thus, SiO2 field and gate **oxide films** were formed on p-Si contg. As-doped n+ layers, SiO2 and Si3N4 (from SiH4-NH3 plasma) films were deposited, the SiO2 and Si3N4 layers were partially **etched** with a CF4-H2 mixt., the damage layer was **etched** off in a CF4-O2 plasma, windows were opened, and the electrodes formed.

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L24 ANSWER 40 OF 40 HCAPLUS COPYRIGHT 2002 ACS
AN 1980:86952 HCAPLUS
DN 92:86952
TI Fabrication of patterned silicon nitride **insulating layers** having gently sloping sidewalls
IN Fogarty, Thomas N.; Harshbarger, William R.; Porter, Roy A.
PA Bell Telephone Laboratories, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 4181564 | A | 19800101 | US 1978-899535 | 19780424 |

AB Amorphous **insulating layers** of Si0.7-1.3N0.7-1.3H3.3-0.7 are deposited in the fabrication of integrated circuits from SiH4-NH3-Ar plasma. The temp. of the substrate surface is decreased during the deposition such that the **etching** rate (in a CF4-O plasma) through the layer is varied to produce windows with sidewalls which are sloped at an acute angle (in particular <60.degree.) with respect to the surface. The initial temp. is 330-375.degree. and the final temp. is 270-325.degree. with a temp. gradient of .gtoreq.2.5.degree./h. Sloped sidewalls permit more complete coverage by a continuous metal layer and ensure contact within a defined area of surface. This method does not require careful control of **etching** time.

L25 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:782154 HCAPLUS
DN 130:46344
TI Nitrided **oxide film** and its manufacture
IN Saito, Hiroshi
PA Central Glass Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 10321620 | A2 | 19981204 | JP 1997-130599 | 19970521 |
| | JP 3221602 | B2 | 20011022 | | |

AB In the film, N concn. decreases from the surface part to the depth direction. The film may contain F. The film is manufd. by fluorinating an **oxide film** with a F compd. and nitriding with a N compd. The film is useful as elec. **insulating films** in manuf. of semiconductor integrated circuits. The film showed improved elec. property and high barrier property to B impurity diffusion.

L32 ANSWER 1 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:172287 HCAPLUS
DN 136:225254
TI Method of etching carbon-containing silicon **oxide films**
IN Hsieh, Chang Lin; Chen, Hui; Yuan, Jie; Ye, Yan
PA Applied Materials, Inc., USA
SO PCT Int. Appl., 19 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI WO 2002019408 | A2 | 20020307 | WO 2001-US26314 | 20010822 |

W: JP, KR, SG
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR

PRAI US 2000-650975 A 20000829
AB The authors discovered a method for plasma etching a carbon-contg. silicon **oxide film** which provides excellent etch profile control, a rapid etch rate of the carbon/contg. silicon **oxide film**, and high selectivity for etching the carbon-contg. silicon **oxide film** preferentially to an overlying photoresist masking material. Then the method of the invention was used, a higher carbon content in the carbon/contg. silicon **oxide film** results in a faster etch rate, at least up to the carbon content of 20 at percent. In particular, the carbon-contg. silicon **oxide film** results in a faster etch rate, at least up to a carbon content of 20 at percent. In particular, the carbon contg. silicon **oxide film** is plasma etched using a plasma generated from source gas comprising **NH3** and CxFy. It is necessary to achieve the proper balance between the relative amts. of **NH3** and CxFy in the plasma source gas to provide a balance between etch by/product polymer deposition and removal on various surfaces of the substrate being etched. The **NH3** gas functions to clean up deposited polzmer on the photoresist surface, on the etched surface, and on process chamber surfaces. The at. ratio of carbon: nitrogen in the plasma source gas typically ranges from .apprx.0.3:1 to .apprx.3:1. C2F6 and C4F8 provide excellent etch rates during etching of carbon-contg. silicon **oxide films**.

L32 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:844914 HCAPLUS
DN 135:379628
TI Method of cleansing vias in semiconductor wafer having metal conductive layer
IN Khosla, Mukul; Tam, Lap; Powell, Ronald A.; Allen, Ronald D.; Rozbicki, Robert T.; Klawuhn, Erich; Settles, E. Derryck
PA Novellus Systems Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6319842 | B1 | 20011120 | US 2001-753432 | 20010102 |

AB Nonvolatile and oxide residues that form during semiconductor processing

are removed from the semiconductor structure in a 2-stage process. An inert gas and a reducing gas are introduced to the reactor. In the 1st stage, the nonvolatile contaminants are sputtered from the semiconductor structure by creating a plasma to ionize the inert gas. The power applied to the plasma is preferably high enough to give the ions of the inert gas a high degree of directionality as they approach the structure. The 1st stage is continued until the nonvolatile contaminants have been sufficiently removed from the structure. In the 2nd stage, the power is reduced and the reducing gas (e.g., H2) reacts with (e.g., Cu oxide) to form elemental metal and H2O vapor. During the 2nd stage there is no appreciable sputtering, and therefore the damage to the structure is limited as compared with processes that use sputtering and redn. simultaneously.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L32 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:128394 HCAPLUS
DN 134:179871
TI Coating materials for sewn products containing adhesives and workability improvers for imparting various functional properties to the sewn products and manufacture of coating materials therefor and coating sewn products with coatings therefrom
IN Sadanari, Shigeyuki; Kimura, Masanao
PA Yuken Chemical K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 2001049581 | A2 | 20010220 | JP 1999-222277 | 19990805 |

AB The coatings essentially contain mixts. (A) comprising adhesives, viscosity adjustors, workability improvers, and color adjusting agents, or the coating materials comprise (A) mixts. contg. softening agents or A mixts. contg. dye discharging agents or A mixts. contg. color developing agents or A mixts. contg. water repellents or A mixts. contg. metals or vapor-deposited metal-coated substances or A mixts. contg. ceramics. Coated sewn products are prepd. by coating sewn products with A mixts. by the roller coating method, spray coating method, or printing method, drying the coating, and hot pressing the coating. Aq. aliph. polyester-polyurethane dispersion 40, di-Me polysiloxane 5, monoethylene glycol 5, monoethanolamine 4, alkyl ether-type nonionic surfactant 2, carbolic acid 0.5, waterborne pigment 4, isocyanate crosslinking agent 4, and H2O 39.5 parts were mixed to give a coating compn. A jean was coated with the coating compn., dried, and hot pressed to give a jean exhibiting leather-like surface and showing good smoothness and luster.

L32 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:863911 HCAPLUS
DN 134:50018
TI Etching of organic **insulation films** for manufacturing of semiconductor devices
IN Kitagawa, Hideo; Suzuki, Nobumasa
PA Canon Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 2000340549 | A2 | 20001208 | JP 1999-153695 | 19990601 |

AB The etching method comprises: introducing a hydrocarbon-contg. treating gas into a container in which a substrate to be treated is placed, supplying elec. energy to form plasma, and etching the org. **insulation film** formed on the substrate. Preferably, the treating gas contains N or H. The semiconductor devices are manufd. by: forming elec.-conductive **layer**, forming **insulation layer**, etching the **insulation layer** by the above method to form desired grooves, and filling the grooves with elec.-conductors.

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L32 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:506086 HCAPLUS
DN 133:98137
TI Oxynitride liner for high reliability with reduced encroachment of the source/drain region in semiconductor device fabrication
IN Gardner, Mark I.; Wristers, Derick; Fulford, H. Jim, Jr.
PA Advanced Micro Devices, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 6093611 | A | 20000725 | US 1997-994502 | 19971219 |

AB A semiconductor process in which a 1st N bearing oxide is formed on an upper surface of a semiconductor substrate. A Si nitride layer is then formed on the N bearing oxide. The 1st N-bearing oxide and the Si nitride layer are then patterned to expose an upper surface of the substrate over a trench region of the substrate. An isolation trench is then etched into the trench region of the substrate and a N bearing liner oxide is then formed on sidewalls and a floor of the trench. An isolation dielec. is then formed within the trench and, thereafter, the Si nitride layer is removed from the wafer. A suitable thickness of the 1st N bearing oxide and of the liner oxide is in the range of .apprx.30 to 100 .ANG.. A consumption of adjacent active regions caused by the thermal oxidn. process is preferably .ltorsim.50 .ANG..
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L32 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:651526 HCAPLUS
DN 129:309476
TI Effects of nitrogen addition to fluorinated silicon dioxide films
AU Hasegawa, Seiichi; Saito, Atsusi; Lubguban, Jorge A.; Inokuma, Takao; Kurata, Yoshihiro
CS Department of Electrical and Computer Engineering, Fac. Technology, Kanazawa University, Kanazawa, 920-8667, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1998), 37(9A), 4904-4909
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English

AB Amorphous fluorinated silicon dioxide (.alpha.-SiO2:F) films doped with nitrogen were deposited by changing the **ammonia** flow rate using plasma-enhanced CVD from SiH4-O2-CF4-**NH3** mixts. The effects of nitrogen addn. to the **films** on both the **dielec.** const. (.epsilon.s) detd. from the capacitance vs. voltage characteristics and the bonding properties examd. by IR absorption measurements, were studied. These results are also discussed in terms of a change in the partial charge on the constituent Si, O, F and N atoms caused by adding F and N atoms to SiO2 films. When .alpha.-SiO2 films are doped by 2-3 at.% with both fluorine and nitrogen under high radiofrequency power and high deposition temp. (Td) conditions, films with low .epsilon.s(.apprxeq. 3.2) and high water resistivity were obtained. Probably Si-F bonds, which act to decrease .epsilon.s value, are stabilized by forming Si-N bonds near the Si-F bonds and by removing weaker Si-F bonds under high radiofrequency power and high Td.

L32 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:863472 HCAPLUS
DN 123:273520
TI Method for fabricating a multilayer semiconductor device
IN Akimoto, Takeshi
PA NEC Corp., Japan
SO Eur. Pat. Appl., 11 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 661736 | A1 | 19950705 | EP 1994-120742 | 19941227 |
| | EP 661736 | B1 | 19990303 | | |
| | R: DE, FR, GB | | | | |
| | JP 07201986 | A2 | 19950804 | JP 1993-336648 | 19931228 |
| | US 5668053 | A | 19970916 | US 1994-364316 | 19941227 |
| PRAI | JP 1993-336648 | | 19931228 | | |

AB The method includes the steps of providing a conductive layer on a substrate; forming a barrier layer on the 1st conductive layer, the barrier layer having a high reflectivity; forming an **insulation layer** on the barrier **layer**; selectively etching the **insulation layer** using the barrier layer as a stopper to form a through-hole; and selectively removing the barrier layer at the bottom of the through-hole from the conductive layer.

L32 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1989:223891 HCAPLUS
DN 110:223891
TI Patterning of thin films in semiconductor device manufacture
IN Morishige, Yukio
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 63176484 | A2 | 19880720 | JP 1987-7583 | 19870116 |

AB The title process in which a pulsed laser is applied to the predetd. region of a thin film (e.g., of phosphosilicate glass) on a substrate

placed in a gas, is characterized in that the gas contains .gtoreq.2 components (e.g., H and O) which can transmit the thin film, and that the gas components react at high temp. to produce heat, or increase their mol. vols. The method can rapidly process thin films without damaging the substrate underneath.

L32 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:206372 HCAPLUS
DN 106:206372
TI Selective and anisotropic dry etching
IN Carbaugh, Susanna Rachel; Stanasolovich, David; Polavarapu, Marty S.; Ng, Hung Yip
PA International Business Machines Corp., USA
SO Eur. Pat. Appl., 12 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI EP 212585 | A2 | 19870304 | EP 1986-111282 | 19860814 |
| EP 212585 | A3 | 19880427 | | |
| EP 212585 | B1 | 19911218 | | |
| R: DE, FR, GB | | | | |
| JP 62052932 | A2 | 19870307 | JP 1986-163940 | 19860714 |
| US 4734157 | A | 19880329 | US 1987-27458 | 19870318 |
| PRAI US 1985-769647 | | 19850827 | | |
| US 1985-769832 | | 19850827 | | |

AB In a method for anisotropically etching poly-Si or silicides with excellent selectivity to an underlying **layer** of Si **oxide** or Si nitride, mixts. of CClF3 or CCl2F2 and **NH3** are employed at moderate pressures in a reactive-ion etching chamber. The method is used in semiconductor device manuf.

L32 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:430065 HCAPLUS
DN 103:30065
TI Silent-discharge gas laser
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 60017975 | A2 | 19850129 | JP 1983-125703 | 19830711 |

AB A cooling medium (e.g., **NH3** or fluorohalocarbon) having a low dielec. const. is sealed in a **dielec.-coated** electrode(s) for a transverse-excited silent-discharge gas laser to effect cooling of the electrode(s) using the heat of vaporization of the cooling medium.

L32 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:184382 HCAPLUS
DN 100:184382
TI Articles produced with multicomponent material
IN Chang, Robert Pang Heng
PA Western Electric Co., Inc., USA

SO Ger. Offen., 41 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | DE 3335107 | A1 | 19840405 | DE 1983-3335107 | 19830928 |
| | DE 3335107 | C2 | 19870423 | | |
| | US 4483725 | A | 19841120 | US 1982-429289 | 19820930 |
| | CA 1209949 | A1 | 19860819 | CA 1983-435235 | 19830824 |
| | FR 2533944 | A1 | 19840406 | FR 1983-15320 | 19830927 |
| | FR 2533944 | B1 | 19891201 | | |
| | GB 2129020 | A1 | 19840510 | GB 1983-25881 | 19830928 |
| | GB 2129020 | B2 | 19860416 | | |
| | NL 8303340 | A | 19840416 | NL 1983-3340 | 19830929 |
| | JP 59084420 | A2 | 19840516 | JP 1983-180923 | 19830930 |
| PRAI | US 1982-429289 | | 19820930 | | |

AB A method of multicomponent film deposition in the fabrication of semiconductor devices and integrated circuits consists of heating the substrate to .ltoreq.250.degree., emitting a flux of neutral particles with a significantly excited fraction into the chamber and emitting other reactive particle fluxes over the substrate. Thus, SiO2 was coated on Si by emitting excited Si atoms and O plasma over a Si substrate.

L38 ANSWER 1 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:483111 HCAPLUS
DN 133:216032
TI Plasma-enhanced chemical vapor deposition Si-rich silicon oxynitride films for advanced self-aligned contact oxide etching in sub-0.25 .mu.m ultralarge scale integration technology and beyond
AU Kim, Jeong-Ho; Yu, Jae-Seon; Ku, Ja-Chun; Ryu, Choon-Kun; Oh, Su-Jin; Kim, Si-Bum; Kim, Jin-Woong; Hwang, Jeong-Mo; Lee, Su-Youb; Kouichiro, Inazawa
CS Bubal-eub, Ami-ri, San 136-1, Semiconductor Advanced Research Division, Hyundai Electronic Industries Co., Ltd., Ichon-si, Kyongki-do, 467-701, S. Korea
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (2000), 18(4, Pt. 1), 1401-1410
CODEN: JVTAD6; ISSN: 0734-2101
PB American Institute of Physics
DT Journal
LA English
AB The authors intentionally introduced excessive Si during the SiOxNy film deposition in order to increase the etch selectivity-to-SiOxNy for advanced self-aligned contact (SAC) etching in sub-0.25 .mu.m ULSI devices. The SiOxNy layer was deposited at a conventional PECVD deposition chamber by using a mixt. of SiH4, **NH3**, N2O, and He. The gas mixing ratio was optimized to get the best etch selectivity and low leakage current. The best result was obtained at 10% Si-SiOxNy. In order to employ SiOxNy **films** as an **insulator** as well as a SAC barrier, the leakage current of the SiOxNy films was evaluated so that SiOxNy may have low leakage current characteristics. The leakage current of a 10% Si-SiOxNy film was 7 .times. 10-9 A/cm2. Besides, the Si-rich SiOxNy layer excellently played the role of antireflection coating for word line and bit line photoresist patterning and sidewall spacer to build a MOS transistor as well as a SAC oxide etch barrier. The contact oxide etching with the Si-rich SiOxNy film was done using **C4F8** /CH2F2/Ar in a dipole ring magnet plasma. As the **C4F8** flow rate increases, the oxide etching selectivity-to-SiOxNy increases, but etch stop tends to happen. The authors' optimized contact oxide etch process showed a high selectivity to SiOxNy larger than 25 and a wide process window (.gtoreq.5 sccm) for the **C4F8** flow rate. When the Si-rich SiOxNy SAC process was applied to a gigabit dynamic RAM of cell array, there was no elec. short failure between conductive layers.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:861490 HCAPLUS
DN 123:244597
TI Formation of silicon nitride thin-films
IN Kobayashi, Naoaki; Urata, Kazuo; Iwasaki, Naoyuki
PA Allied Materials, Inc., USA
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 07201847 | A2 | 19950804 | JP 1993-332407 | 19931227 |
| | JP 07099744 | B4 | 19951025 | | |

AB The process involves (1) impressing a high-frequency 1st power on a NF3-contg. reactive gas for cleaning the inside-wall of a deposition chamber by plasma-etching, (2) impressing a 2nd power on a **NH3** -contg. reductant gas for removing a F-contg. residual such as NF3, CF3, and/or **C2F6** from the surface of the chamber, (3) impressing a high-frequency 3rd power on a feed gas contg. SiH4, **NH3**, and/or N2, and (4) subsequently impressing a high-frequency 4th power on the activated feed gas. The process provides deposition of Si nitride interlayer insulators with smooth and tight films in prevention of excess-Si-contg. film formation.

L38 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:844387 HCAPLUS
DN 123:260630
TI Cost-effective ultrahigh-pure gas delivery system in clean rooms
AU Dubey, G. C.; Purohit, R. K.
CS Solid State Physics Laboratory, Delhi, 110054, India
SO Proc. - Inst. Environ. Sci. (1995), 41st(Contamination Control), 500-8
CODEN: IESPAF; ISSN: 0073-9227
DT Journal
LA English
AB Ultrahigh-pure gases are required in various application in processing in clean rooms for electronic device fabrication. The management of gas delivery system should be such that it would need least disturbance and particle generating activity. Also as the toxic gases are involved in the processing, the operator confidence should be improved by indicating the gas pressure etc. near the site of operation. Most of the gases are pyrophoric and therefore proper fire protection is also necessary. The design aspect of gas delivery system choice of various components for such system in a cost effective manner is described. The case is discussed for a fab line of GaAs devices where the gases like **NH3**, SiH4, BCl3, Cl2, H2, CH4, **CF4**, etc. are being used for deposition of Si nitride **films** for capping **dielec**. and passivation, etching of Cr mask, etching of GaAs for via holes, etc. Various safety aspects are also discussed.

L38 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:602002 HCAPLUS
DN 113:202002
TI **Insulating** transparent materials **coated** with carbon films
IN Yamazaki, Shunpei; Hayashi, Shigenori; Ishida, Noriya; Sasaki, Mari; Takeyama, Junichi
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 02104665 | A2 | 19900417 | JP 1988-255492 | 19881011 |
| | JP 2775263 | B2 | 19980716 | | |
| | JP 2000226665 | A2 | 20000815 | JP 2000-56704 | 19881011 |
| | JP 3256212 | B2 | 20020212 | | |
| | JP 2000226666 | A2 | 20000815 | JP 2000-56705 | 19881011 |
| | JP 2000226662 | A2 | 20000815 | JP 2000-56706 | 19881011 |
| | JP 3254202 | B2 | 20020204 | | |
| | JP 2000226663 | A2 | 20000815 | JP 2000-56707 | 19881011 |

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|---|---|---|---|---|---|
| | JP 2000226664 | A2 | 20000815 | JP 2000-56708 | 19881011 |
| | JP 2002115061 | A2 | 20020419 | JP 2001-230363 | 19881011 |
| | JP 10180925 | A2 | 19980707 | JP 1997-365049 | 19971220 |
| | JP 2923275 | B2 | 19990726 | | |
| | JP 11286778 | A2 | 19991019 | JP 1999-19780 | 19990128 |
| | JP 3057072 | B2 | 20000626 | | |
| PRAI | JP 1988-255492 | A3 | 19881011 | | |
| | JP 1997-365049 | A3 | 19881011 | | |
| | JP 1999-19780 | A3 | 19881011 | | |
| | JP 2000-56705 | A3 | 19881011 | | |

AB The material is coated with a C-base hydrophilic film and <5 .times. 1013 .OMEGA.-cm in sp. resistivity. The C film is hydrogenated-fluorinated and contains trivalent or pentavalent elements. A diamond-like C primer film 100-2000-.ANG. thick was formed on an org. material from C2H2 and a diamond-like C film was formed thereon from **C2F6**, H2, and **NH3** by plasma chem. vapor deposition.

L38 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:469075 HCAPLUS
DN 107:69075
TI Low dielectric constant amorphous silicon boron nitride (SiBN) ternary films prepared by plasma-enhanced deposition
AU Maeda, Masahiko; Makino, Takahiro
CS Electr. Commun. Lab., NTT, Tokai, 319-11, Japan
SO Jpn. J. Appl. Phys., Part 1 (1987), 26(5), 660-5
CODEN: JAPNDE
DT Journal
LA English
AB Novel **insulator films** named amorphous SiBN ternary films were studied. The films were prepd. by plasma-enhanced chem. vapor deposition using a SiH4-B2H6-**NH3**-Ar mixt. The dependences of the film properties on film compn. were investigated. These **films** show good **insulation** characteristics and conformal step coverage. These films can be easily etched by reactive ion etching using H2/**CF4** gas mixt. A very low dielec. const. lower than that of SiO2 is realized when the B at. ratios are beyond 0.30. BN shows hygroscopic properties while stability to moisture is confirmed for SiBN films. Therefore, SiBN films will be applicable as interlayer insulation in a low parastic capacitance multilevel metalization.

L38 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:431003 HCAPLUS
DN 103:31003
TI Characterization of a new substrate for tunneling spectroscopy
AU Gauthier, S.; De Cheveigne, S.; Salace, G.; Klein, J.; Belin, M.
CS Group. Phys. Solides l'ENS, Paris, F-75251, Fr.
SO Surf. Sci. (1985), 155(1), 31-45
CODEN: SUSCAS; ISSN: 0039-6028
DT Journal
LA English
AB An **insulating layer** is produced on Al by a glow discharge in **CF4**. This substrate, used as the insulator of metal-insulator-metal diodes is characterized by IETS as AlF3. The adsorption of **NH3**, benzylamine, and formic and propiolic acids on this substrate is investigated. A comparison between the spectra of samples obtained on this insulator and on alumina for the same dopant mols. shows significant differences which are interpreted as revealing an enhanced Lewis acidity of AlF3 relative to Al2O3, detd., at least in part, by an enhanced electroneg. of surface Al+ cations of AlF3.

L38 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:230473 HCAPLUS
DN 102:230473
TI Apparatus and method for plasma-assisted electron-beam evaporation
IN Nath, Prem
PA Energy Conversion Devices, Inc., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI US 4514437 | A | 19850430 | US 1984-606014 | 19840502 |
| CA 1242165 | A1 | 19880920 | CA 1985-479799 | 19850423 |
| EP 161088 | A1 | 19851113 | EP 1985-302864 | 19850424 |
| EP 161088 | B1 | 19880608 | | |
| R: CH, DE, FR, GB, IT, LI, NL | | | | |
| JP 60243268 | A2 | 19851203 | JP 1985-94556 | 19850501 |
| JP 04075314 | B4 | 19921130 | | |
| PRAI US 1984-606014 | | 19840502 | | |

AB An improved method and app. are described for depositing thin films, such as In Sn oxide, onto substrates. The deposition comprises one step in the fabrication of electronic, semiconductor, and photovoltaic devices. An electron beam vaporizes a source of solid material, and electromagnetic energy provides an ionizable plasma from reactant gases. By passing the vaporized solid material through the plasma, it is activated prior to deposition onto the substrate. In this manner, the solid material and the reactant gases are excited to facilitate their interaction prior to the deposition of the newly formed compd. onto the substrate. The solid material may be In, Sn, Cd, Zn, Ti, Si, Ge, or their mixts. The reactive gas may be O2, N2, **NH3**, CH4, H2S, N2O, **CF4**, or their mixts. The process is specifically adapted for the deposition of transparent conductive **oxide films**, e.g., In Sn oxide and Sn **oxide**, onto amorphous semiconductor **layers**. The films are electrodes in photovoltaic devices, e.g., solar cells.

L38 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:104584 HCAPLUS
DN 102:104584
TI Silicon nitride films for dynamic RAMs
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 59169142 | A2 | 19840925 | JP 1983-42340 | 19830316 |

AB Si3N4 films suitable for dynamic RAMs are prepd. at high growth rates by forming a discharge in a gas contg. N and F compds. to directly nitride the surface and then thermally depositing Si3N4 from a gas contg. Si and N compds. Thus, a Si substrate was exposed to a **CF4**-N2 mixt. in a discharge at 1.3 kW to form a thin nitride layer and then SiH2Cl2 and **NH3** were added at 900.degree. to form the Si3N4 film.

L38 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS

AN 1984:149222 HCAPLUS
DN 100:149222
TI Insulation degradation and anomalous etching phenomena in silicon nitride films prepared by plasma-enhanced deposition
AU Maeda, Masahiko; Nakamura, Hiroaki
CS Atsugi Electr. Commun. Lab., Nippon Telegr. and Teleph. Public Corp., Atsugi, 243-01, Japan
SO Thin Solid Films (1984), 112(3), 279-88
CODEN: THSFAP; ISSN: 0040-6090
DT Journal
LA English
AB The dependence was studied on the deposition conditions of **insulation** degrdn. obsd. in **films** produced by plasma-enhanced chem. vapor deposition (PECVD) and used as interlayer insulation. The Si3N4 films were deposited using 2 different parallel-plate electrode reactors at 13.56 MHz. The gas mixts. employed were SiH4-N2 or SiH4-**NH3**, with or without Ar gas as a diluent, or SiH4-**NH3**-N2. Regardless of the gas mixts. used, all films exhibited excellent step coverage. However, Cu decoration revealed that films prepd. using a gas system contg. Ni show a high d. of field-induced insulation defects at the boundaries between the flat and side portions of films over the substrate steps. These boundaries exhibit anomalous etching phenomena in a buffered HF soln. or a **CF4** plasma. Films prepd. using the N2-free gas system show excellent insulation yield and no anomalous etching phenomena.

L38 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1981:126135 HCAPLUS
DN 94:126135
TI Preventing corrosion of aluminum and aluminum alloys
IN Iida, Shinya; Ueki, Kazuyoshi; Mizutani, Tatsumi; Komatsu, Hideo; Hirobe, Kado
PA Hitachi, Ltd., Japan
SO Eur. Pat. Appl., 15 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 19915 | A1 | 19801210 | EP 1980-102980 | 19800528 |
| | EP 19915 | B1 | 19840919 | | |
| | R: DE, GB, NL | | | | |
| | JP 55158275 | A2 | 19801209 | JP 1979-65030 | 19790528 |
| | JP 56017434 | B4 | 19810422 | | |
| | US 4308089 | A | 19811229 | US 1980-148283 | 19800509 |
| PRAI | JP 1979-65030 | | 19790528 | | |

AB Atm. corrosion of Al and Al alloys after dry etching in a halogen-contg. gas is prevented by (1) sputtering in a **NH3**-contg. atm. (2) washing with a liq. The treatment is useful in the manuf. of semiconductor devices. Thus, an Al-4Cu-2%Si [51195-02-9] film 2 .mu.-thick was formed on a Si substrate having a thermal **oxide film** 0.6 .mu.-thick. After masking with a photoresist to give the desired pattern, the specimen was dry etched in BCl3(g) at 24 Pa and 13.56 MHz, and sputtered in **CF4**(g) at 20 Pa and 0.2 W/cm2 in a diode-type app. After removal of the **CF4**, the specimen was similarly sputtered in **NH3** at 40 Pa for 1.5 min. After adding N to restore atm. pressure, the specimen was removed, dipped in a HNO3 soln. to remove residual Cu, washed 2 min in a NH4OH soln., and water washed 5

min. No corrosion occurred in the Al alloy lines 2-3 .mu.-wide even during subsequent processing.

L38 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1977:544869 HCAPLUS
DN 87:144869
TI Semiconductor device
IN Yonezawa, Toshio; Ishida, Hidekuni; Hiraki, Shunichi; Kitane, Shoichi
PA Tokyo Shibaura Electric Co., Ltd., Japan
SO Ger. Offen., 14 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | DE 2654689 | A1 | 19770616 | DE 1976-2654689 | 19761202 |
| | DE 2654689 | C2 | 19861023 | | |
| | JP 52067970 | A2 | 19770606 | JP 1975-144255 | 19751203 |
| | JP 59022381 | B4 | 19840526 | | |
| | GB 1536003 | A | 19781213 | GB 1976-50319 | 19761202 |
| | US 4155802 | A | 19790522 | US 1976-746898 | 19761202 |
| | FR 2334206 | A1 | 19770701 | FR 1976-36576 | 19761203 |
| | FR 2334206 | B1 | 19801017 | | |
| PRAI | JP 1975-144255 | | 19751203 | | |

AB In the manuf. of transistors, after conventional doping steps, all masks are completely removed, and an **insulating** SiO2 **layer** of apprx.1500 .ANG. is formed by exposure to H-O-C2HCl3 or H-O-HCl. This is covered by a apprx.1000 .ANG. Si3N4 layer from reaction of SiH4 with **NH3**, which is selectively etched with H3PO4 or **CF4** -plasma to leave the areas above the separator, base, emitter, and resistance regions covered. By using the remaining Si3N4 as a mask, a 2nd SiO2 layer of 5000-6000 .ANG. is formed by a similar process to the 1st, the remaining Si3N4 is recovered by etching, the total surface is covered with a 2000-4000 .ANG. SiO2 layer and a 2000-3000 .ANG. P- or P-As-doped SiO2 layer, and electrodes are introduced. The resulting transistor produces less noise and spurious signals and can withstand higher voltages than conventional transistors.